19.3 A MEMS-Based Dynamic Light Focusing System for Single-Cell Precision in Optogenetics

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Optogenetics is a technique that involves the use of light to excite or inhibit neurons that have been genetically modified to express light-sensitive ion channels (opsins). Implanted LEDs or optical fibers are the most common approaches in optogenetic stimulation systems, but their broad illumination and lack of beam steering capability make them insufficient for probing individual neurons. When a 3D scanning optical system is used to control the position of a laser spot, single-cell precision can be achieved in a volume of tissue containing millions of cells. Due to the sub-ms response time of modern opsins and a demand for high throughput neural stimulation [1], a random-access scanning system requires a kHz refresh rate, and the capability to dwell on a target depth for an arbitrary length of time. Existing lateral (XY) scanning tools are fast, however state-of-the-art axial (Z) scanning technologies such as electrically tunable lenses (ETLs) [2] and liquid crystal (LC) lenses [3] are limited to >3ms settling times. Alternative axial scanning tools either lack dwelling capability [4] or have impractical actuator drive requirements [5].

We propose an axial focusing device comprised of an ASIC and phase modulating piston-motion MEMS mirrors with settling times <100µs [6] enabling a 10kHz refresh rate. The driver ASIC is capable of addressing MEMS process variations that impact voltage-to-displacement behavior by employing a nonlinear, reconfigurable 6-bit DAC to achieve a linear input code-to-displacement response. We combine the driver with a 23,852-element MEMS array wired as 32 independently addressable rings to demonstrate high-speed axial (Z) focusing capability. The ASIC also has a 200×200 pixel array with pad openings that can drive 40,000 independent MEMS mirrors at a 10kHz refresh rate to serve as a development platform for a MEMS mirror-based spatial light modulator (SLM), which would unify all three axes of scanning in a single, integrated device and would enable high-speed 3D optogenetic control of up to thousands of neurons [7].

Figure 19.3.1 shows a photograph of the fabricated mirror array with a rendering of one electrostatically activated piston-motion mirror structure and its properties. We have designed and fabricated the array using the MEMSCAP PolyMUMPs process with thickness modifications and custom Au lift-off post-processing [6]. Each micromirror pixel consists of a fixed bottom electrode that, through parallel-plate capacitive voltage-based transduction, actuates an electrically biased mirror body supported by two clamped-guided suspension beams. Pixel-level phase shifting is achieved as the travel path of incident light is increased by an amount that corresponds to twice the mirror actuation displacement. The mirrors have a nonlinear displacement vs. actuation voltage curve (Fig. 19.3.1) given by the equation

$$V(\Delta z) = \sqrt{a(b-\Delta z)^2\,\Delta z} \qquad (1)$$

where a and b are fit parameters, and are susceptible to process variations, requiring per-part calibration. Commercial drivers utilize high-resolution DACs to calibrate the devices post-fabrication by forming lookup tables. This solution inefficiently utilizes high-resolution DACs even though high precision is only required for a small portion of the actuation curve. Since V(Δz) is nonlinear, a linear DAC wastes dynamic range (and data rate) in the region of the curve where the transduction gain is low, and hence a higher voltage LSB can be used. By reusing the precision setting elements of a DAC as sample and hold capacitors for voltages that correspond to each input code, a nonlinear DAC can save area and power compared to a linear DAC approach.

Figure 19.3.2 shows the simplified block diagram of the driver ASIC. The nonlinear DAC generates 64 voltages that correspond to linearly spaced mirror displacement levels. A 4Gbps LVDS link consisting of four channels, each operating at 1Gbps with 6b/8b encoding is used to transmit mirror displacement data for the pixel array, which is scanned into a shift register chain to configure analog multiplexers and select corresponding analog voltages to be written to each pixel's DRAM cell. Each unit pixel contains a single pad opening to bond a MEMS mirror and two capacitors that comprise an analog DRAM cell. 32 of these pixels are connected to output buffers to drive the internal voltages off-chip to an external MEMS die.

Figure 19.3.3 shows the schematic of the nonlinear DAC, which employs a 6-bit current integration-based programmable reference voltage generator. A capacitor bank containing 64 unit capacitors (C_{UNIT}=2.2pF), a current source for controlled discharge, and a reset switch are all connected to a common node. Initially, all capacitors are reset to V_{RESET}=8V, and then discharged through the current source (I_{BIAS}=2µA). Capacitors are sequentially disconnected from the common node to sample voltages that correspond to their respective codes. Timing is controlled by a state machine and on-chip memory containing discharge times for each code (8 bits/code) that are multiplied by (50ns) to yield . The generated voltage for a given code i is $V_i = V_{i+1} - (I_{BIAS} \times \Delta T_i / C_{TOT}(i))$ where $C_{TOT}(i)$ is the total capacitance connected to the discharge node for each code. As capacitors are removed from the common node, discharge speeds up and precision of the generated voltage decreases. The programmability simultaneously cancels mirror nonlinearity and calibrates process variations. Figure 19.3.3 also shows the timing diagram with the generation and retention of voltage levels for two possible nonlinear actuation curves. Voltages are then buffered with rail-to-rail class AB amplifiers and distributed to the analog multiplexers. Due to the leakage of stored charge on the capacitors to the bulk of the switch devices, the nonlinear DAC is refreshed every 2.5ms, keeping drift <0.5LSB error in mirror position.

Pixels are laid out in a 200×200 array format with 22.5µm pitch, each with a pad. Figure 19.3.4 shows the schematic and operation of the DRAM write chain containing analog multiplexers, an auto-zeroing line driver to buffer the DAC voltage, and the unit pixels containing five switches, two MOM capacitors (250fF) and a pad opening for driving individual mirrors (C_{mirror}~10fF). To avoid rolling shutter artifacts, a global-shutter mode is used with the MOM capacitors under ping-pong operation: while C_{d1} is connected to the pad driving the MEMS device, C_{d2} is overwritten to store the next frame. With the trigger of a new frame, the capacitors switch roles and C_{d2} is used to drive the pad openings while the subsequent frame's values are written to C_{d1}.

The IC was fabricated in TSMC's 40nm HV CMOS process and dissipates a total of 308mW with the power breakdown shown in Fig. 19.3.7. Figure 19.3.5 shows static and dynamic measurement results, taken using a digital holographic microscope (DHM). Static measurements show a post-calibration max(DNL) and max(INL) of 0.19LSB and 1.14LSB, respectively, where 1LSB is 3.9nm. Dynamic measurements show max 10-90% rise and fall times of 80µs and 82µs, respectively. The setup and results for axial focusing measurements are shown in Fig. 19.3.6. Focused spot positions were determined from peak intensities in the target volume. Some deviations from the aimed depths were observed due to aberrations in the optical system, which can be calibrated through aiming at pre-distorted depths. With a 100mm lens, volumetric efficiency (VE) = $Energy_{spot}/Energy_{FoV}$ was measured to be 38% at the focal plane with a focal tuning range of ±10mm.

Figure 19.3.7 shows the ASIC micrograph, performance summary and comparison table of currently used axial focusing solutions (ETL and LCoS) with two high-speed chip-scale approaches (DMDs and this work) that have >36× higher speed. Compared with DMDs, this work offers 10× higher VE, 10× lower power, and uses ~33× fewer actuators.

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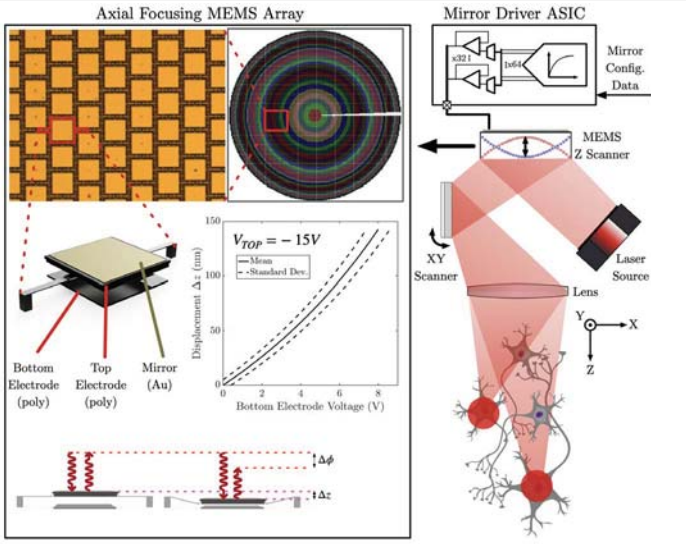


Figure 19.3.1: Diagram of a MEMS-mirror based axial focusing system with an XY scanner demonstrating a compact 3D scanning system for single-cell resolution optogenetics.

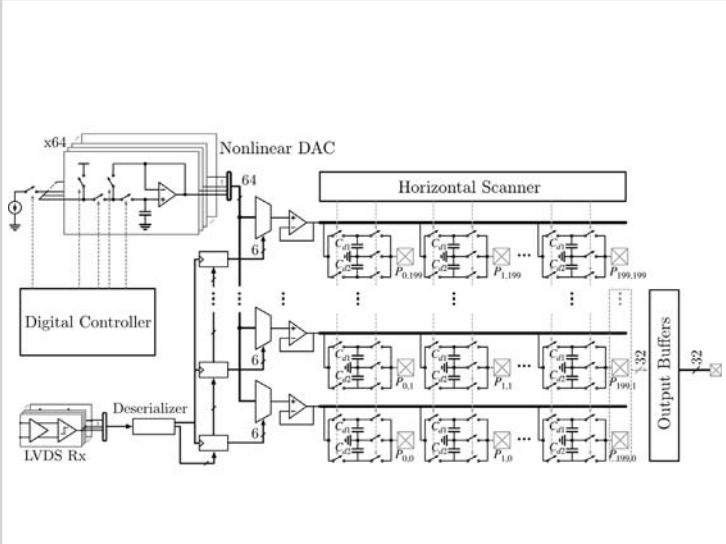


Figure 19.3.2: Simplified IC block diagram with MEMS pad openings denoted as $P_{i,j}$. Output Buffers are connected to 32 of the pixels in the last column.

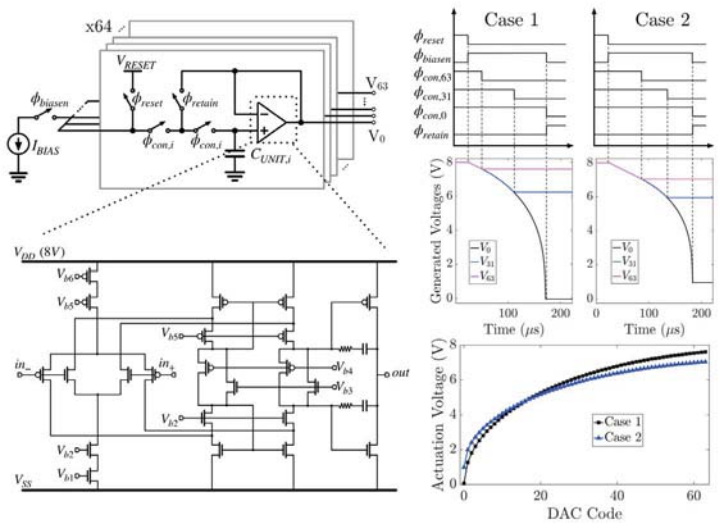


Figure 19.3.3: Schematic of the nonlinear reconfigurable DAC and the rail-to-rail class AB amplifier buffering the stored voltages. Measured results from two example cases of voltage generation depicting different actuation curves.

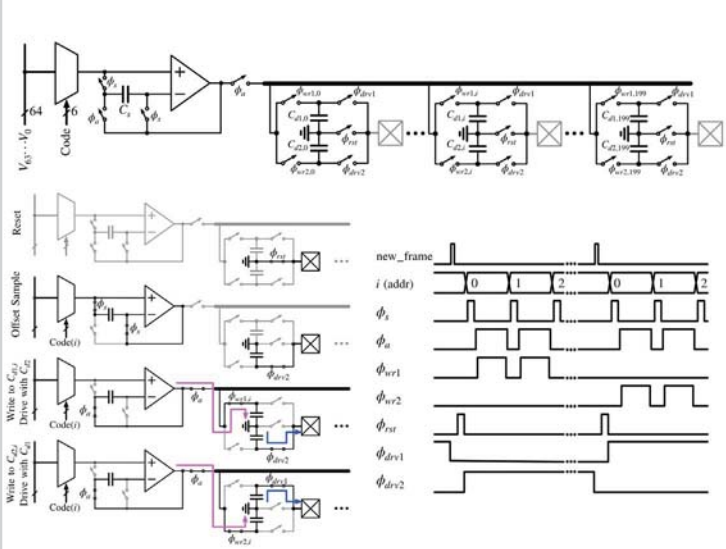


Figure 19.3.4: DRAM write chain for a single row showing states of operation.

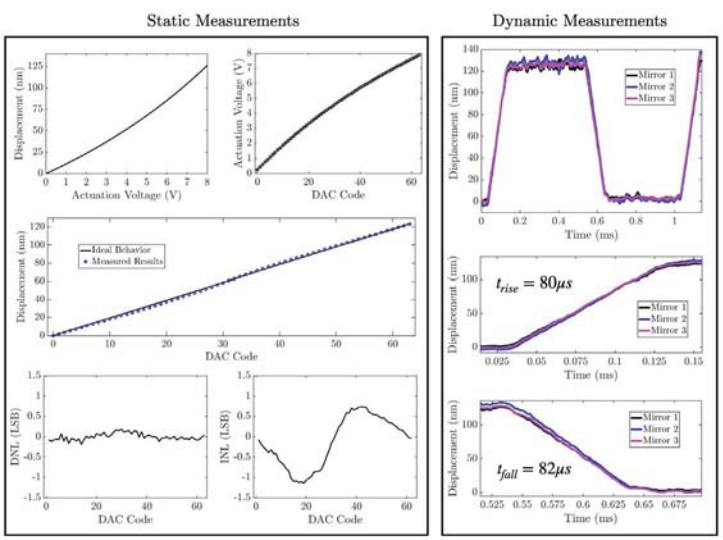


Figure 19.3.5: Static and dynamic measurements of the MEMS+ASIC system.

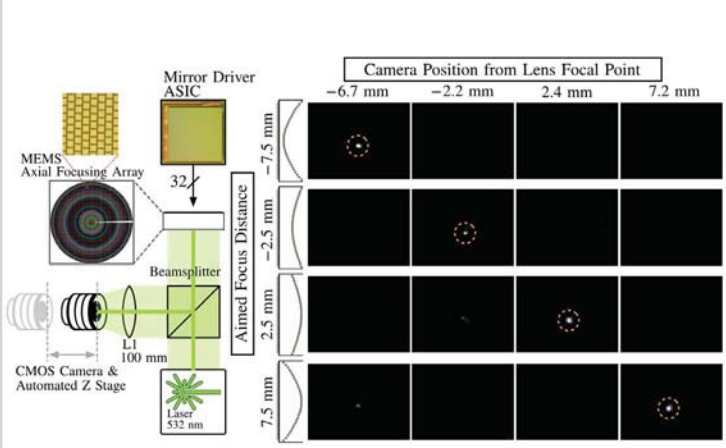
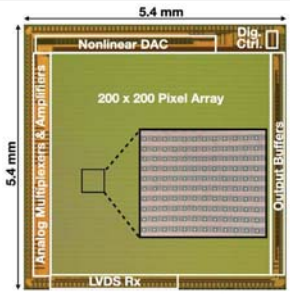


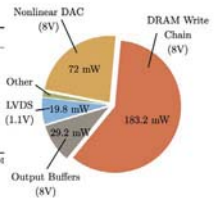
Figure 19.3.6: Optical measurement setup for the ASIC driving the axial focusing micromirror array and z-stack measurements relative to background illumination for four target focus depth configurations.



Driver ASIC Specifications

	This work
Technology	40nm + HV
Refresh Rate	10kHz - 2MHz*
Pixel Array Size	200×200
Pixel Pitch	22.5 μm
Drive Voltage Range	0-8 V
Actuation Resolution	6 bits
Power Consumption	308 mW

* 10 kHz for the entire array, 2 MHz for the 32 buffered outputs



Axial Focusing Systems Comparison Table

	[2]	[3]	[8]	This work
Actuator Type	ETL	LC Lens	DMD	Piston Mirror
Settling Time*	>15 ms	>3 ms	45 μs	82 μs
Volumetric Efficiency**	N/A†	>90%	3.7%	38%
Number of Actuators	–	–	786k	24k
Number of Independent Channels	–	–	786k	32
IC Power Consumption	–	–	2-4.4 W	308 mW
Required Datarate	–	–	25.6 Gbps	3 Mbps

* 10% to 90% settling time
** Measured at the focal plane
† ETLs are not diffractive devices

Figure 19.3.7: Chip micrograph with pad openings shown in the inset, chip specifications, power consumption breakdown, and axial focusing systems comparison table.

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