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SUPPLEMENTARY INFORMATION

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A wireless and artefact-free 128-channel neuromodulation device for closed-loop stimulation and recording in non-human primates

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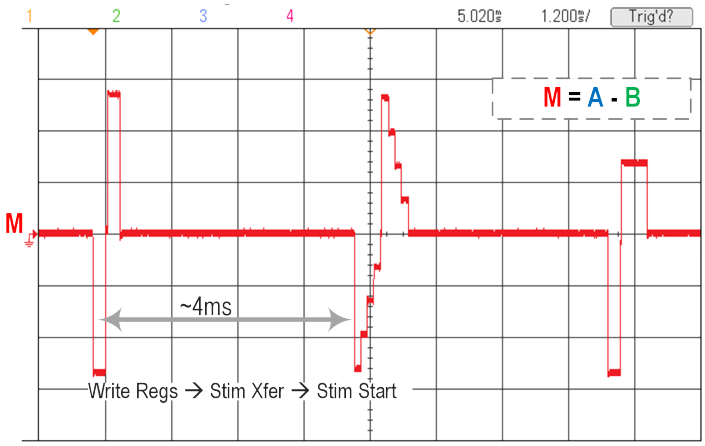
NMIC stimulator programmability

Parameter	Value	Unit
Stimulation subsystem		
Nominal supply voltage	3, 6, 9, or 12	V
Stimulation compliance	11.8	V
Number of stimulation units	4	
Number of addressable channels	66	
Stimulation settings		
Stimulation current resolution	20, 40, 60, or 80	µA
Maximum stimulation current	5.04	mA
Pulse resolution	15.625	µs
Maximum pulse width	500	µs
Interphase gap	31.25-1000	µs
Short time	31.25-1000	µs
Frequency	15-255	Hz

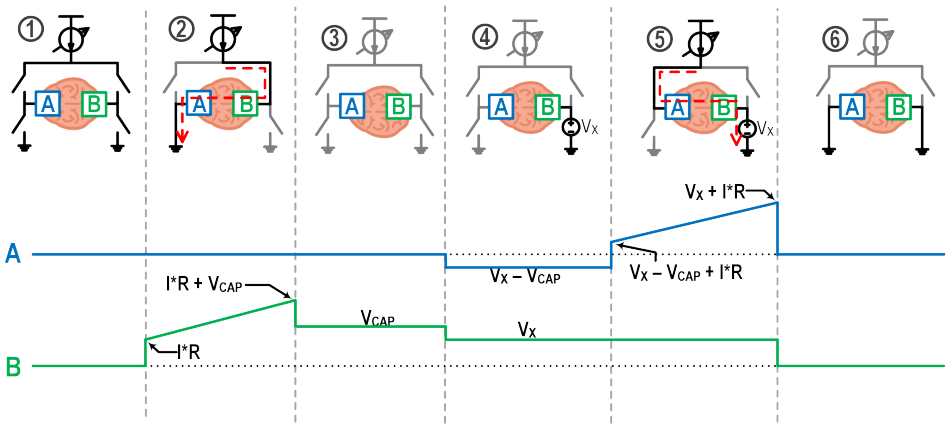


Supplementary Figure 1 – NMIC stimulator parameters and rapid waveform update. A table including stimulator subsystem specifications and settable stimulation pulse parameters is shown on the left. Rapid waveform reconfiguration between pulses delivered at the maximum frequency (255 Hz) is demonstrated on the right. Stimulation parameters can be updated every pulse. Additionally, multiple current sources can be multiplexed to a single electrode to create higher amplitude stimulation or complex waveforms, for example.

System artifact resiliency

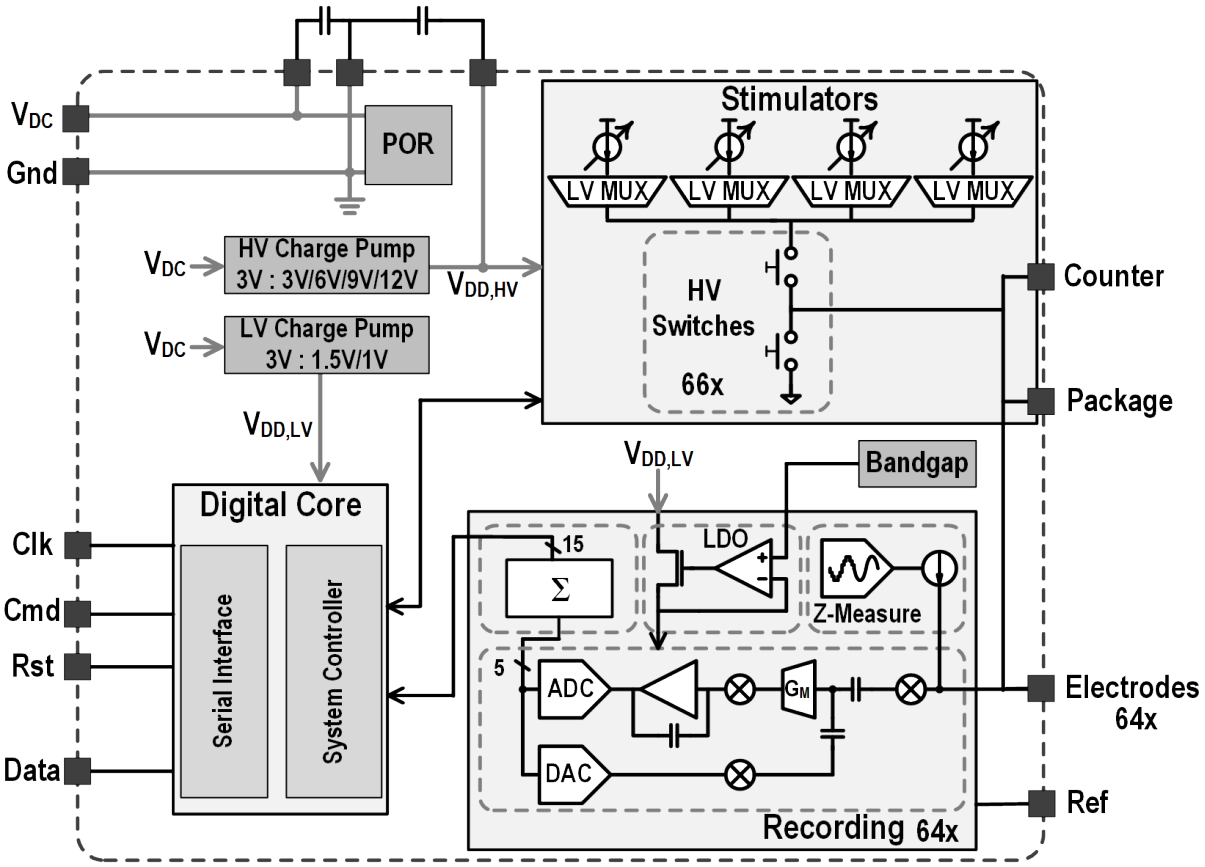
Methods implemented on the NMIC for preventing and mitigating stimulation artifact are described here. While the NMIC itself does not completely remove stimulation artifacts, it avoids saturation and minimizes artifact duration to make back-end cancellation more manageable.

In order to prevent large, persistent artifacts, biphasic stimulation pulses should be used instead of monophasic pulses. Following a single-phase stimulation pulse, a second phase pulse with opposite polarity is delivered to actively clear the charge delivered during the first pulse. The amount of indirect artifact is related to the amount of residual charge left over after both phases. The NMIC stimulator architecture prevents large indirect artifacts from occurring by ensuring accurate charge balance between the biphasic pulses and also enabling passive discharge through shorting of electrodes. Common methods for charge-balancing stimulation pulses include current copying[78,79], current driver feedback control[26], and voltage offset correction through feedback[80]. The NMIC employs an H-bridge architecture allowing the reuse of the same current source during both phases of stimulation, eliminating the effects of process, voltage and temperature (PVT) variations and achieving 0.016% mismatch between phases (**Supplementary Fig. 2**)[27,45,81]. Further details can be found in the NMIC paper[27].



Supplementary Figure 2 – H-bridge stimulator timing diagram. The stimulator reuses the current source for both stimulation phases to achieve precise phase matching. The voltage offset, Vx, is used during the second phase to prevent the voltage on either electrode from going negative. A shorting phase of programmable duration is used to clear any residual charge on the electrodes.

Because the NMIC integrates the stimulators and front-ends onto the same chip, a common ground reference is shared between these two subsystems (**Supplementary Fig. 3**). This provides an additional benefit that, during passive discharge following a stimulation pulse, the stimulation electrodes are shorted to the reference voltage of the front-ends.



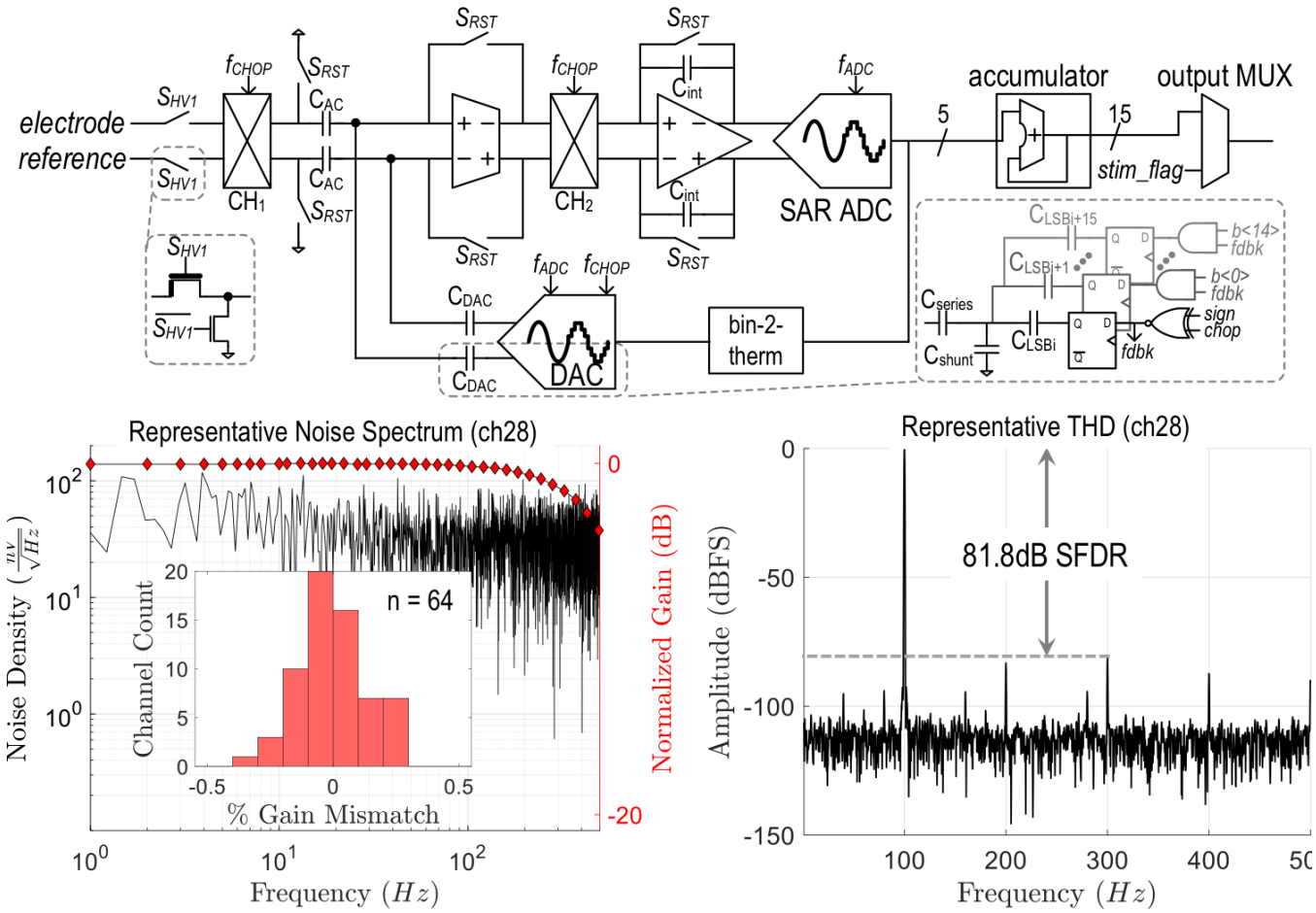
Supplementary Figure 3 – system architecture of the NMIC. The NMIC enables a bidirectional neural electrode interface with integrated stimulation, recording, impedance measurement, and power management. The NMIC uses a reference electrode as a common reference for sensing. The counter and package electrodes can be used as additional simulation channels and are unused in this work.

Large direct artifacts and remaining indirect artifacts can saturate front-end amplifiers with small input ranges. Techniques for mitigation of stimulation artifacts at the recording front-end fall into two categories: saturation prevention and rapid recovery[82]. Saturation prevention can be achieved by increasing dynamic range or by subtracting artifact signals in the analog domain. Subtraction of learned artifacts can reduce the voltage swings at the amplifier input, but current implementations still allow residual artifacts to pass through due to error in the subtracted artifact templates[48,49]. Alternatively, designers can increase the amplifier input ranges to tolerate larger signal swings without subtraction[22,27,47]. Rapid recovery methods reduce artifacts due to charge build-up of components in the front-end circuit, with resetting capacitive elements in the front-end being a common method[26,27,50,51]. A more complex implementation involves active discharging of these elements[83]. The NMIC implements a front-end architecture that provides both a large input range and rapid recovery between samples[27].

The NMIC front-end uses a first order, continuous-time, incremental (resetting) ADC with capacitive feedback to achieve a large input range (**Supplementary Fig. 4**). The forward signal path consists of an active integrator and a 5-bit successive approximation register (SAR) ADC. By bringing the ADC inside the amplifier's capacitive feedback loop, internal signal swings are reduced, resulting in improved linearity. The analog forward path filters the SAR residue providing first order quantization noise shaping, which is approximately 6 dB (1 bit of resolution) per doubling of oversampling frequency. The SAR is oversampled 1024 times resulting in a nominal resolution of 15 bits at 1 kS/s. A reset occurs every output sample using the switches labeled S_{RST}. Every sample is memoryless and therefore rapidly recovers from a saturating signal.

The input range is defined by the closed-loop capacitive ratio and the voltage supply of the feedback digital-to-analog converter (DAC; 930 mV). On each side of the front-end, the input capacitance is 1.6 pF and the effective feedback capacitance is 86 fF, or approximately 2.8 fF per bit of feedback from the DAC. A capacitive attenuation network is used to achieve a feedback capacitance smaller than unit size (31 fF) to improve matching. The input range is calculated as 930 mV · 86 fF / 1.6 pF = 50 mV for each polarity, which is 100 mVpp. A setting to change the capacitance ratio results in an input range of 400 mVpp, which can be used in rare cases when artifact amplitudes exceed 50 mV amplitudes.

This large, linear input range allows the NMIC to record artifacts 10's of mV in amplitude without saturating, while simultaneously recording small neural signals with low noise. The noise level of the front-end is dominated by the thermal noise of the analog forward path and the quantization noise of the converter (nominally about 950 nV_{rms} each, input-referred). Flicker noise of the analog forward path would dominate by an order of magnitude; however, the forward path uses a chopper to up-modulate the flicker noise of the transconductance stage, which is filtered by the integrator.



Supplementary Figure 4 – architecture of the recording front-end and measurement results. The frontend is an incremental oversampled converter with 15-bit nominal resolution and is DC-coupled. The front-end resets every sample (1ms) which aids in rapid recovery from stimulation artifact. Noise spectrum is input-referred and SFDR spectrum from a single channel is normalized to full scale input ($100mV_{pp}$, f_{in} = 100Hz, SNDR = 76.7dB). Measurements were taken once from a single representative channel (ch28). All system circuits were active during measurements and the outputs were taken from digital bit stream.

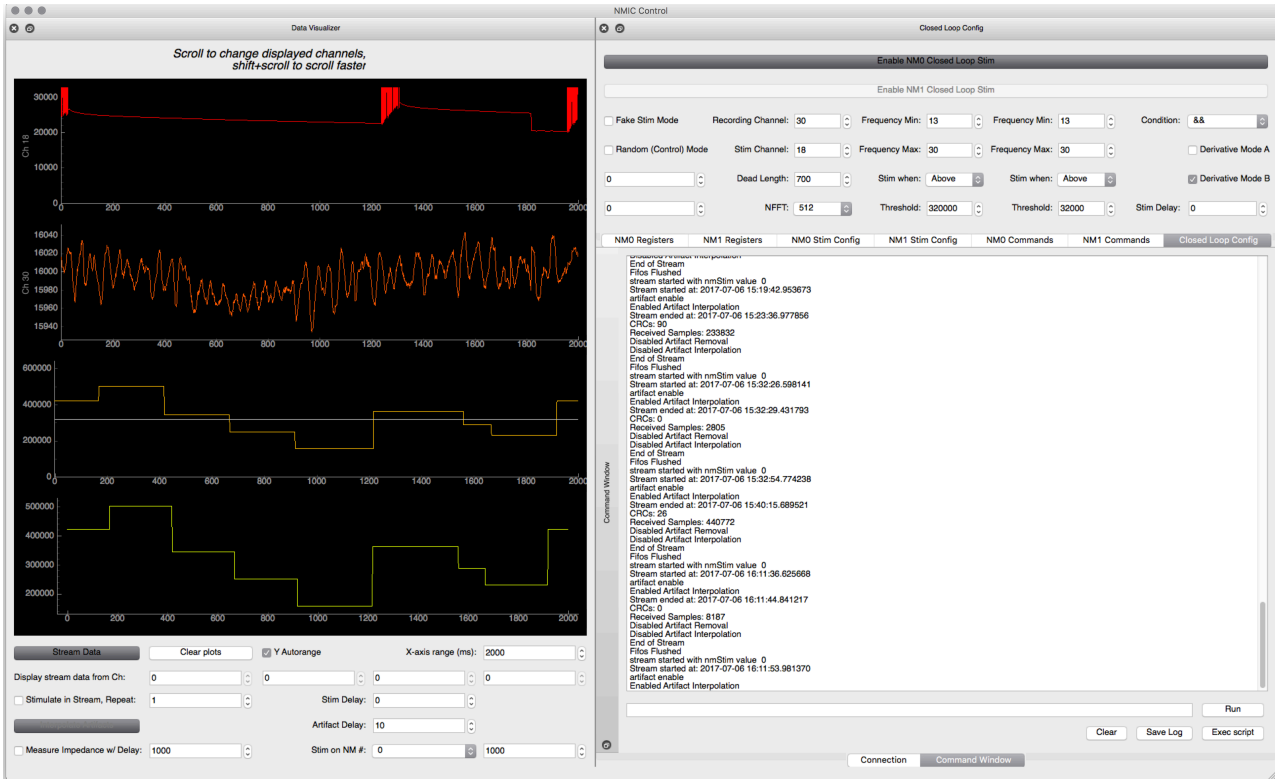
A comparison of fully integrated, bidirectional neural interfaces with an emphasis on artifact prevention and mitigation is given in **Supplementary Table 1**.

Supplementary Table 1 – A comparison of bidirectional neural interface ICs

	Rhew JSSC '14[25]	Chen JSSC '14[26]	Shulyzki TBioCAS '15[45]	Mendrela JSSC '16[48]	Kassiri JSSC '17[22]	Johnson VLSI '17[27]
Process technology (nm)	180	180	350	180	130	180HV
No. channels (rec/stim)	4/8	8/1	256/64	8/4	64/64	64 / 4**
ADC resolution	8	10	8	10	--	15
ENOB	5.6	9.57	5.1	--	11.7	12.45
Sampling rate (samples/s/ch)	25k	62.5k	15k	4k	1k*	1k
Power/channel (µW)	61.25	58	52	0.33	0.63	8
IR noise (nV/rtHz)	81	63	113	68	51	68§
CMRR (dB)	--	--	60	--	89	85
Input range (mVpp)	1.2	10	--	10*	--	100 / 400
THD	0.8% (1.2mVpp)*	--	0.8% (1mVpp)	--	--	0.012% (100mVpp)
Stim max amplitude	4.2 mA / 5 V	30 µA / 10 V	250 µA / 2.6 V	--	1.35 mA / 3.1 V	5.04 mA** / 12 V
Input coupling	AC-coupled	AC-coupled	AC-coupled	AC-coupled	Rail-to-rail DC	±50mV / ±200mV DC
Biomarker Computation	Logarithmic DSP, LFP energy PI controller	FFT, ApEn, LLS classifier DSP	Off-chip‡	--	Phase-synchrony DSP	Off-chip†
Wireless data streaming	2.4 GHz backscatter	MedRadio band OOK	Off-chip‡	--	UWB	Off-chip†
Power supply	915 MHz RF harvesting + 5V battery	13.56 MHz inductive link	Battery‡	--	1.5 MHz inductive link	Battery†
Artifact duration (ms)	--	--	--	2 (assumed)	--	1
Artifact prevention	--	Current driver feedback controller	Current driver reuse for balancing	--	Passive discharge, stimulator matching	Compatibility, current source reuse for balancing, passive discharge
Artifact mitigation	--	Saturation detection and rapid recovery	--	Adaptive filter artifact subtraction, common averaging reference	Rail-to-rail DC offset	High dynamic range, rapid recovery

* Estimated
** All four stimulators can be combined on a single channel for 20.16mA
§ Average noise across channels is 77nV/rtHz
† System described in this work
‡ System described in main comparison table

Graphical user interface



Supplementary Figure 5 – screenshot of WAND GUI running a closed-loop experiment. The left side of the window is dedicated to real-time data visualization. From the top, the traces are of one of the stimulation channels, the control channel, and two calculated biomarkers with thresholds shown as a horizontal line. In this case, the two bottom traces appear to show the same information because the both the raw value and the time derivative of the same biomarker were used. Full power spectrums were calculated on the device and transmitted to the GUI, where local integration of band power was performed before visualization. The right side of the window contains settings for the closed-loop experiment and a command shell for displaying data stream information.