An Energy-Efficient Miniaturized Intracranial Pressure Monitoring System

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***Abstract*— A miniaturized pressure-sensing microsystem targeting intracranial pressure monitoring is presented. The system takes full advantage of Invensense MEMS-CMOS process to heterogeneously integrate the sensor and interface. This integration type requires no fabrication postprocessing and results in sub-pF sensor-interface parasitic interconnection capacitance C_p which is an order of magnitude smaller than previously reported C_ps. Since energy efficiency is of main concern, the minimum energy consumption for maintaining a certain signal-to-noise ratio (SNR) is analytically calculated and compared for two energy-efficient sensor front ends, namely, the switched-capacitor (SC) capacitance-to-voltage converter (CVC) and the successive approximation register (SAR) capacitance-to-digital converter (CDC). The comparison reveals for small values of C_p and for low-to-moderate SNR, the SAR CDC outperforms the SC CVC in terms of power consumption. Heterogeneous integration of sensor and CMOS electronics results in only 720 fF of C_p which enables direct SAR capacitance-to-digital conversion. Correlated double sampling is also integrated into the proposed SAR switching scheme to combat $1/f$ noise and the input-referred offset voltage of the comparator. The entire pressure-sensing system measures 2.2 × 2.6 × 0.4 mm^3 in size, consumes 130 nW at 60-Hz sampling rate, and obtains 57-dB SNR with 0.2% sensor-electronics combined linearity over 520-mmHg pressure range.**

***Index Terms*— Capacitive pressure sensor, correlated double sampling (CDS), energy-efficient, intracranial pressure (ICP), Invensense, noise, optimization, successive approximation register (SAR) capacitance-to-digital converter (CDC), switched-capacitor (SC).**

I. Introduction

CEREBRAL blood flow (CBF) must be maintained at a constant level (∼50 mL of blood per 100 g of brain tissue per minute [1]) to ensure a sustained delivery rate of oxygen and nutrients to brain cells. Low levels of CBF results in irreversible brain ischaemia, permanent disability, or death. Brain autoregulation mechanism adjusts CBF for a wide range of cerebral perfusion pressure (CPP) (∼60–160 mmHg). Analogous to Ohm's law, CBF is defined by

$$\mathrm{CBF} = \frac{\mathrm{CPP}}{\mathrm{CVR}} \tag{1}$$

where CPP is cerebral perfusion pressure, and CVR is cerebrovascular (flow) resistance. Cerebral autoregulation counteracts CPP variations by modulating CVR accordingly, which is done through the dilation and constriction of cerebral vessels in response to, respectively, decreased and increased CPP. As a result, CVR tracks CPP, and CBF remains relatively constant. CPP, however, may depart the autoregulatory range of brain for various reasons, such as traumatic brain injury (TBI). In the case of TBI, due to the swelling of brain, intracranial pressure (ICP), that is the pressure of cerebrospinal fluid (CSF), increases significantly which results in a proportional decrease to CPP because for the high levels of ICP, CPP = MAP − ICP, where MAP is the mean arterial blood pressure. So, elevated levels of ICP (>20 mmHg) indirectly slows down CBF and results in life-threatening brain ischaemia. Thus, *continuous* ICP monitoring followed by the external drainage of CSF in the case of raised ICP is recommended after all medium to severe head injuries.

Current *in situ* methods of ICP monitoring include intraventricular catheter, fiber-optic catheter tip transducer [2], and microchip transducer [3]. For these methods, skull is drilled and a catheter is guided inside the cranium. The catheter is connected to an external readout device during measurement. Because the cranium is exposed, infection rate escalates (>∼%5–15) hindering prolong (in the order of months) continuous ICP measurement. Furthermore, because of the sensitivity of catheters to movement and elevation, the mobility of patients is restricted. This has limited ICP monitoring only to emergency conditions. In fact, the correlation between ICP and common nonemergency symptoms, e.g., headache, is not well studied due to lack of a simple technique capable of prolong continuous ICP measurement in a normal medium rather than intensive care units.

Portrayed in Fig. 1 is the cross section of the heterogeneously integrated MEMS-CMOS pressure sensor proposed for continuous ICP monitoring [4]. The final device will include an RF power scavenging circuitry for power/data transmission. Nonetheless, this paper focuses only on the data acquisition subsystem. The device measures 0.4 mm in thickness thin enough [5] to be implanted in the subarachnoid

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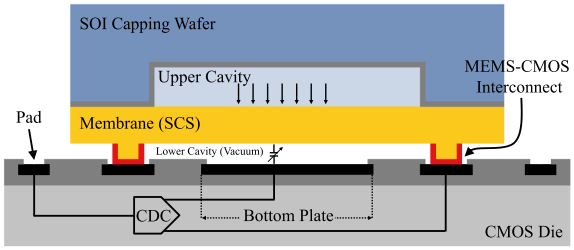

Fig. 1. System cross section.

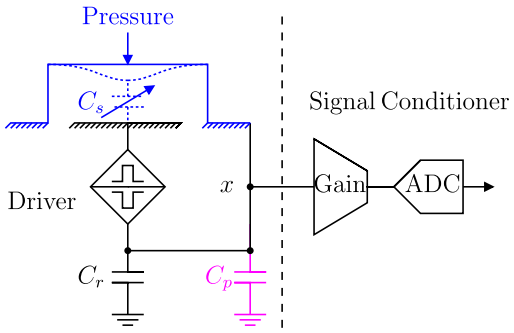

Fig. 2. Generic capacitive pressure-sensing system.

TABLE I
STANDARD AND TARGETED REQUIREMENTS OF ICP MONITORING DEVICES

	Range [mmHg]	Accuracy [mmHg]	Resolution [mmHg]	BW [Hz]	Power [uW]
Standard	0–20 20–100	±2 10%	<4	>30	N/A
Target	0–(100,200)	±2	1–4	50	<1

space. As the device dimensions decrease, the available power drops proportionally. Thus, to maximize the lifetime of the implant, special attention is paid to energy efficiency of the system.

According to the Association for the Advancement of Medical Instrumentation (AAMI) [6], an ICP monitoring device should have a pressure range of 0–100 mmHg, ±2 mmHg accuracy in the range of 0–20 mmHg, and a maximum error of 10% in the range of 20–100 mmHg. Furthermore, ICP waveforms can have frequency components up to 15 Hz [7]. This mandates sampling rates of greater than 30 Hz. No minimum detectable pressure is prescribed by AAMI, however, to meet the accuracy requirement, pressure resolution should be better than 4 mmHg. These requirements along with targeted specifications are listed in Table I.

For the absence of any static power consumption at the driving side of the interface, capacitive sensing is adopted. Choosing the right sensor-interface architecture is not evident by surveying the state-of-the-art since a significant number of capacitive sensor interfaces reported in the literature are designed for energy-relaxed industrial applications [8]–[23], and there are few which focus on low-power designs [24]–[34]. Furthermore, none of the reported interfaces are a *sensor-specific* design. In fact, they are all general purpose sensor front ends. But, in this paper, there is a great deal of flexibility in codesigning the sensor and interface. This, as discussed in Section III, relaxes some design requirements of the interface. Thus, the energy-efficiency evaluation of available sensor interfaces is performed through circuit analysis. Section II provides a background on the topic and introduces the concept of holistic noise-power optimization for sensor interfaces. Then, in Section III, the proposed noise-power optimization technique is applied to the well-known switched-capacitor (SC) and successive approximation register (SAR) sensor interfaces to compare their energy efficiencies. Section IV describes the mechanical structure of the sensor, and Section V reviews the design of the correlated double sampling (CDS) SAR capacitance-to-digital converter (CDC) used in the system. Measurement results are summarized in Section VI, and the conclusions are drawn in Section VII.

II. HOLISTIC NOISE-POWER OPTIMIZATION

Shown in Fig. 2 is a generic pressure sensor interface comprised of a driver and a signal conditioner. Unlike data converters, a sensor interface needs to both *generate* its signal and condition it. Due to manufacturing challenges, differential capacitive pressure sensors are scarce [35], [36]. A reference capacitor C_r is commonly used to offset the base capacitance C_{s0} of the sense capacitor $C_s = C_{s0}+\Delta C$. Moreover, the sensing element is usually wire-bonded to the interface leading to a problematic parasitic capacitance at the interconnection node.

The driver is responsible for generating the signal by extracting ΔC from the sense capacitor. This requires deposition of charge in C_s and C_r. Only a fraction, depending on the topology and the sensor sensitivity $\Delta C/C_{s0}$, of the energy consumed for charging C_s and C_r contributes to the power of the generated signal P_{signal} at the input of the conditioning circuit. So, P_{signal} can be related to the power consumption of the driver P_{driver} by

$$P_{\text{signal},x} = \eta \times P_{\text{driver}} \tag{2}$$

where $\eta \leq 1$ is an efficiency factor. As an example, consider a half-bridge capacitive driver, Fig. 3. The signals ϕ_1 and ϕ_2 are nonoverlapping clocks with frequency f. If the output signal is defined as the total amount of charge flowing into node x during ϕ_2, P_{signal} and the average consumed charging power are, respectively

$$P_{\text{signal}} = (\Delta C \times V_{\text{ref}})^2 \tag{3}$$

$$P_{\text{driver}} = f(C_s + C_r){V_{\text{ref}}}^2. \tag{4}$$

So, for a fixed ΔC, increasing P_{signal} commands increasing V_{ref} which proportionally increases P_{driver}.

In Fig. 2, noise at node x $P_{\text{noise},x}$ is dominated by the input-referred noise of the signal conditioning block which in turn

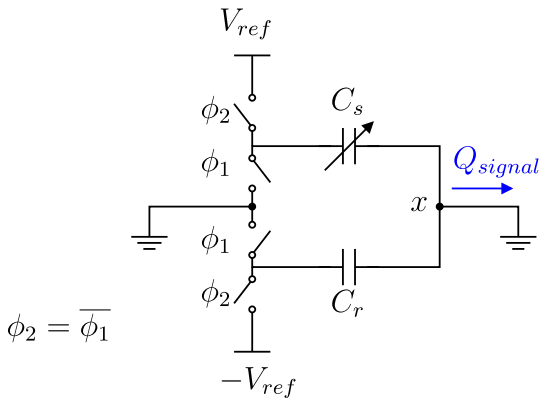

Fig. 3. Half-bridge capacitive sensor driver.

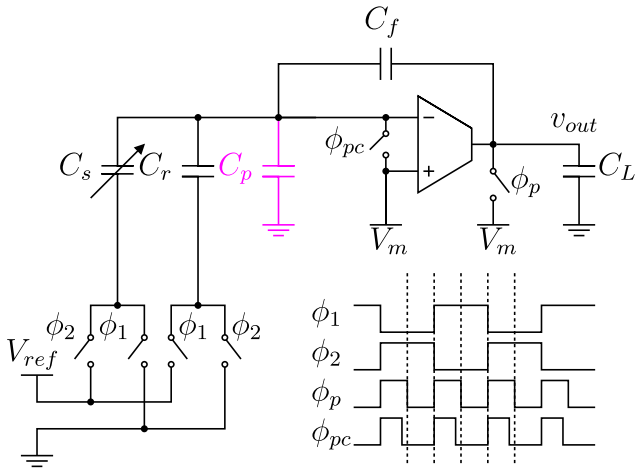

Fig. 4. SC CVC schematic.

is inversely proportional to its power consumption $P_{\text{conditioner}}$, that is,

$$P_{\text{noise},x} \propto (P_{\text{conditioner}})^{-1}. \tag{5}$$

Dividing (2) by (5), the signal-to-noise ratio (SNR) at node x is found as

$$\text{SNR}_x = \frac{P_{\text{signal},x}}{P_{\text{noise},x}} \propto (P_{\text{driver}} \times P_{\text{conditioner}}). \tag{6}$$

So, as long as the product of P_{driver} and $P_{\text{conditioner}}$ is constant, a certain SNR can be achieved. A family of solutions then exists for power allocation, though only one solution is optimal which minimizes

$$P_{\text{total}} = P_{\text{driver}} + P_{\text{conditioner}}. \tag{7}$$

By converting the proportionality of (6) to equality by the constant factor K, the optimal solution will be

$$P_{\text{driver}} = P_{\text{conditioner}} = \sqrt{\frac{\text{SNR}}{K}}. \tag{8}$$

In general, (6) is oversimplistic and fails to appropriately model the dependencies of SNR, P_{driver}, and $P_{\text{conditioner}}$. Therefore, for topologies of interest, the actual relationships between (P_{driver}, P_{signal}) and ($P_{\text{conditioner}}$, P_{noise}) can be analytically derived, and optimal P_{driver} and $P_{\text{conditioner}}$ can be found in a similar fashion exemplified earlier. In Section III, the introduced optimization technique is applied to the SC capacitance-to-voltage converter (CVC) and the SAR CDC to enable a comparison between the two.

III. Architectures of Interest

The SC integrator basically converts sense capacitance (change) to voltage [8]. A literature review indicates that it is the most favored sensor front end, upon frequency of reports, for capacitive sensor measurements [8]–[24], [32], [33], [37]–[39], and thus is an architecture of interest for the analysis that follows.

The superb energy efficiency of SAR analog-to-digital converters hints at the possibility that the SAR CDC can potentially reach the same level of energy efficiency. The direct SAR CDC [40] is blamed for its poor performance in handling large parasitic capacitance C_p. For the SAR CDC, offsetting C_p demands increasing P_{driver}, however, bypassing it via an SC CVC requires raising $P_{\text{conditioner}}$. We examine the energy efficiency of the two architectures and critically compare their performance in the presence of arbitrary C_p. The SC interface is treated first. Note that the SC CVC produces an analog output, while the SAR output is already digitized. So, to make the comparison as fair as possible, it is assumed that the SC CVC is followed by a state-of-the-art ADC for numerical performance comparison.

A. SC CVC

The schematic of the SC CVC is shown in Fig. 4. Precharged CDS switching scheme [41] is used as a reference architecture since it requires only a single supply rail (in contrast to bipolar $\pm V_{\text{ref}}$ supply rails [8]) and enables digital correction of low-frequency noise and the input-referred offset of the amplifier V_{OS}. The signals ϕ_1 and ϕ_2 are two nonoverlapping conversion clock signals, while ϕ_p defines the precharging phase. A complete CVC cycle requires two precharging phases each followed by a voltage conversion phase. The operation of the SC CVC is summarized in Fig. 5. At the end of the first and second conversion phases, the output voltage of the amplifier is, respectively

$$v_{o1} = \frac{C_s - C_r}{C_f} V_{\text{ref}} + \frac{C_s + C_r + C_p}{C_f} V_{\text{OS}} \tag{9}$$

$$v_{o2} = \frac{C_r - C_s}{C_f} V_{\text{ref}} + \frac{C_s + C_r + C_p}{C_f} V_{\text{OS}}. \tag{10}$$

It is assumed that at the end of each phase, $v_{o1,2}$ is digitized. So, subtracting (9) from (10) in the digital domain yields

$$v_{\text{signal}} = v_{o1} - v_{o2} = \frac{2\Delta C}{C_f} V_{\text{ref}}. \tag{11}$$

The power consumption of the half-bridge driver for a full conversion cycle can be expressed as

$$P_{\text{driver}} = f_s (C_s + C_r) {V_{\text{ref}}}^2 \tag{12}$$

where f_s is the conversion frequency. Two noise sources contribute to the total output referred noise $\overline{v_n^2}$ of the SC CVC,

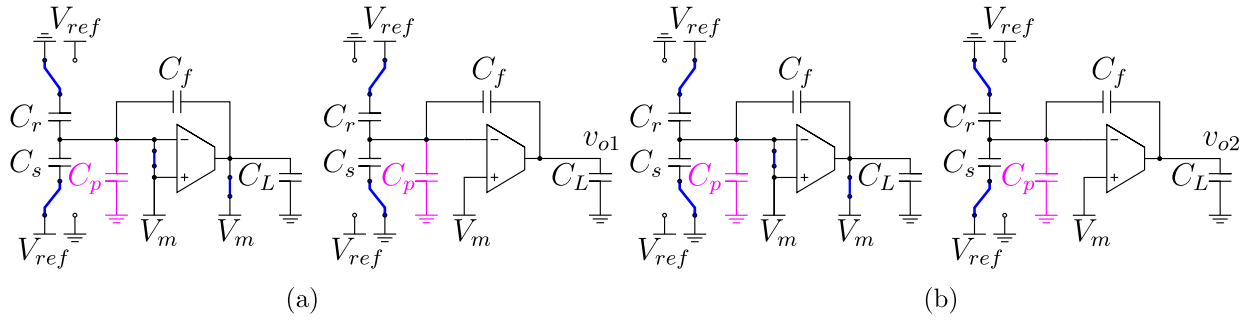

Fig. 5. SC CVC conversion phases. (a) First precharge, subconversion. (b) Second precharge, subconversion.

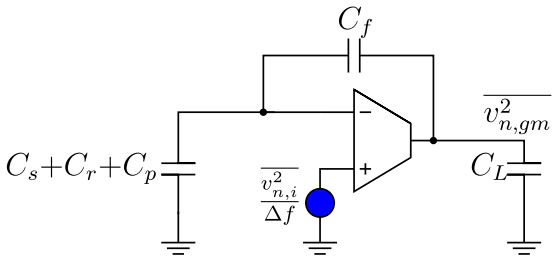

Fig. 6. SC CVC diagram for the purpose of noise analysis of the conversion period.

$\overline{v_n{}^2} = 2(\overline{v_{n,\mathrm{sw}}{}^2} + \overline{v_{n,\mathrm{gm}}{}^2})$, where $\overline{v_{n,\mathrm{sw}}{}^2}$ is due to the noise of the switches during the precharging phase, $\overline{v_{n,\mathrm{gm}}{}^2}$ is regarding the noise of the amplifier during the conversion phase, and the factor of 2 is due to double sampling. Just before ϕ_{pc} transitions to low, C_s, C_r, C_p, and C_f appear in parallel and form a single degree of freedom from energy storage point of view. Based on the equipartition theorem [42], the total noise charge sampled by this degree of freedom will be $\overline{q_n{}^2} = kT(C_s + C_r + C_p + C_f)$, where k and T are Boltzmann's constant and absolute temperature, respectively. The noise charge $\overline{q_n{}^2}$ redistributes across C_f in the conversion phase and generates

$$\overline{v_{n,\mathrm{sw}}{}^2} = \frac{kT(C_s + C_r + C_p + C_f)}{{C_f}^2}. \tag{13}$$

Fig. 6 shows the SC CVC in the conversion period. The amplifier is modeled by a g_m-cell with unit-gain bandwidth g_m/C_L. During this phase, only the amplifier noise is considered, because if the switches are designed with ON-resistance $R_{\mathrm{ON}} \ll 1/g_m$, their noise contribution to $\overline{v_n{}^2}$ is minimal and can be ignored [42]. The noise transfer function $V_{n,\mathrm{gm}}/V_{n,i}$ and the output noise power $\overline{v_{n,\mathrm{gm}}{}^2}$ during the conversion phase are respectively

$$\mathrm{NTF}(s) = \frac{1}{\beta\left(1 + s\frac{C_L+(1-\beta)C_f}{\beta g_m}\right)} \tag{14}$$

$$\overline{v_{n,\mathrm{gm}}{}^2} = \frac{kT\gamma\alpha/\beta}{C_L + (1-\beta)C_f}. \tag{15}$$

In (14) and (15), $\beta = C_f/(C_s+C_r+C_p+C_f)$ is the feedback factor, γ is the noise coefficient of MOS transistors, and α is the topology-dependent excess noise factor of the amplifier. The total output noise power is then

$$\overline{v_n{}^2} = \frac{2kT(C_s + C_r + C_p + C_f)}{{C_f}^2} + \frac{2kT\gamma\alpha/\beta}{C_L + (1-\beta)C_f}. \tag{16}$$

Assuming the duration of the precharging phase is negligible to that of the conversion phase, if $f_s = 1/T_s$ is the sampling frequency, the output of the amplifier has $T_s/2$ s to settle to within half-LSB error, so

$$v_o e^{-T_s/2\tau} \leq \frac{v_o}{2^{N+1}}. \tag{17}$$

In (17), $\tau = 1/\omega_{-3dB}$ is the time constant of the system in the conversion phase, and N is the quantization resolution. Solving (17) for τ finds the minimum bound on the system bandwidth

$$\omega_{-3dB} \geq f_s(N+1)\ln(2). \tag{18}$$

Based on (16), increasing C_L is the only way to decrease $\overline{v_n{}^2}$, because other terms are either constants (K, T, γ, and α) or given by the sensor specifications and interconnection quality [C_s, C_r, C_p, and C_f due to (11)]. Increasing C_L, however, tradesoff with ω_{-3dB} and ultimately g_m [according to (18)] through

$$\omega_{-3dB} = \frac{\beta g_m}{C_L + (1-\beta)C_f}. \tag{19}$$

Combining (11), (16), (18), and (19), the relationship between the SNR, V_{ref}, and g_m can be expressed as

$$g_m = \frac{\alpha\gamma f_s(N+1)\ln(2)}{\frac{2}{kT\,\mathrm{SNR}}\left(\frac{\Delta C V_{\mathrm{ref}}}{C_s+C_r+C_p+C_f}\right)^2 - \frac{1}{C_s+C_r+C_p+C_f}}. \tag{20}$$

Depending on the topology and biasing regime of the amplifier, g_m can be related to its power consumption. For instance, for a subthreshold folded-cascode amplifier

$$P_{\mathrm{amplifier}} \geq 2\zeta V_t g_m V_{\mathrm{dd}} \tag{21}$$

where ζ is the subthreshold slope coefficient and V_t is the thermal voltage. For a list of design parameters (C_s, ΔC, C_p, f_s, V_{dd}, α, γ, and SNR), (20) finds a family of solutions for V_{ref} and g_m. Each solution duo (V_{ref} and g_m) can then be mapped to the power consumption domain (P_{driver}, $P_{\mathrm{amplifier}}$, and P_{total}) according to (7), (12), and (21). In case the

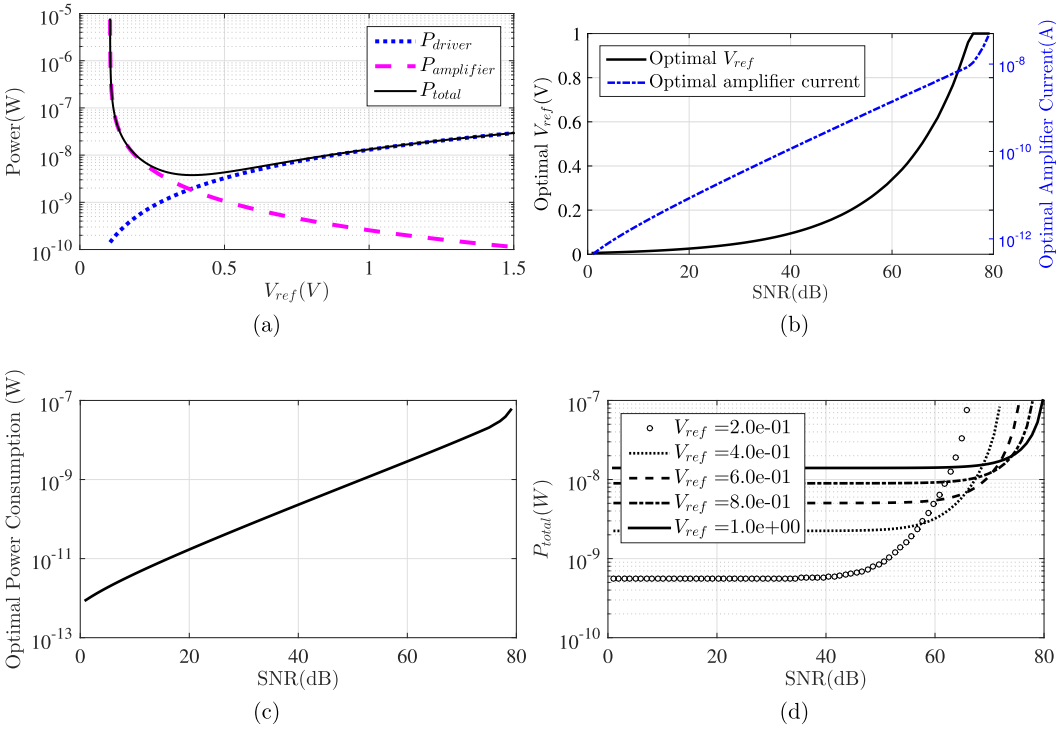

Fig. 7. Noise-power optimization of the SC CVC. (a) Power management of subblocks of the SC CVC for the case of 60 dB SNR. (b) Optimal V_{ref} and amplifier current. (c) Lower bound on P_{total}. (d) Total power consumption of the interface for different driving voltages.

TABLE II
TYPICAL DESIGN PARAMETERS USED FOR NOISE-POWER OPTIMIZATION OF SC CVC AND SAR CDC

C_{s0}	ΔC	C_p	α	γ	ζ	V_{dd}	f_s
6[pF]	2[pF]	6[pF]	4	0.5	1.5	1[V]	1000[Hz]

SC CVC is followed by an ADC, $P_{\text{amplifier}}$ must be offset by the power consumption of the ADC, P_{ADC}.

Table II lists typical design parameters used for the illustration of noise-power optimization of the SC CVC. To achieve 60 dB of SNR, Fig. 7(a) shows the family of solutions for power allocation. Total power consumption of the interface is also plotted in the same panel suggesting that for 60 dB of SNR, P_{total} is minimized only if $V_{\text{ref}} = 0.38$ V. For a given SNR, there exists a unique V_{ref} (and so $I_{\text{amplifier}}$) that leads to a minimal P_{total}. These values are shown in Fig. 7(b) where it is assumed that the maximum available voltage is 1 V (the same as V_{dd}). For SNR $>$ 75 dB, V_{ref} is capped to 1 V. So, to maintain the required SNR, the amplifier noise must be more aggressively reduced which needs a significant increase in its supply current. Following the results shown in Fig. 7(b), the lower bound on P_{total} as a function of SNR can be derived as shown in Fig. 7(c). To avoid the complexity of generating an arbitrary V_{ref}, $V_{\text{ref}} = V_{\text{dd}}$ can be used. To illustrate the excess power consumption, in this case, consider Fig. 7(d). Choosing $V_{\text{ref}} = V_{\text{dd}} = 1$ V, instead of the optimal value of 0.38 V, when 60 dB of SNR is required gives rise to a P_{total} which is five times as large as the theoretical minimum.

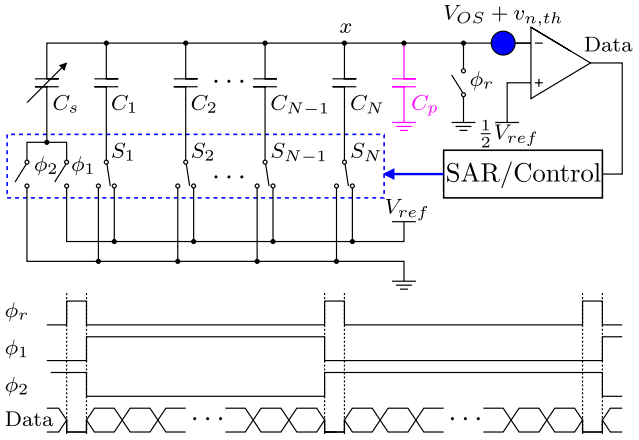

Fig. 8. SAR CDC architecture.

B. SAR CDC

The SAR CDC architecture is shown in Fig. 8. To make the power consumption comparison of the two interfaces as fair as possible, the SAR CDC analyzed here also incorporates CDS. Furthermore, we assume that the comparator is comprised of a latch and a preamplifier, and the noise and the offset of the preamplifier dominate.

The interface operates in two phases ϕ_1 and ϕ_2. Each phase is preceded by a reset phase ϕ_r during which all the capacitors are discharged. In ϕ_1, the bottom plate of the sense capacitor C_s is switched to V_{ref} and the bottom plates of the capacitors in the capacitive array are switched to V_{ref} in a SAR fashion such that at the end of ϕ_1, the input terminals

of the comparator are at the same potential, neglecting the quantization error, that is,

$$V_{\text{ref}}\frac{C_s + C_{\phi_1}}{C_s + C_p + C_T} + (V_{\text{OS}} + v_{n,\text{th}}) = \frac{1}{2}V_{\text{ref}} \quad (22)$$

where C_T is the total capacitance of the array, $C_{\phi 1}$ is the total capacitance of the array that remains connected to V_{ref} at the end of ϕ_1, V_{OS} and $v_{n,\text{th}}$ are, respectively, the offset and the input-referred thermal noise of the comparator. Rearranging (22), $C_{\phi 1}$, which is available in the digital domain, is given by

$$C_{\phi 1} = \frac{C_T - C_s + C_P}{2} - \frac{V_{\text{OS}} + v_{n,\text{th1}}}{V_{\text{ref}}}(C_T + C_s + C_p). \quad (23)$$

In ϕ_2, the bottom plate of C_s is connected to ground, and the SAR bit-cycling process results in

$$C_{\phi 2} = \frac{C_T + C_s + C_P}{2} - \frac{V_{\text{OS}} + v_{n,\text{th2}}}{V_{\text{ref}}}(C_T + C_s + C_p). \quad (24)$$

The final digital code C_{out}, in terms of capacitance, is found by subtracting (23) from (24) which has a signal component $C_{\text{out},s}$ and a noise component $C_{\text{out},n}$ as

$$C_{\text{out}} = C_s + \frac{v_{n,\text{th1}} - v_{n,\text{th2}}}{V_{\text{ref}}}(C_T + C_s + C_p) \quad (25)$$

$$C_{\text{out},s} = C_s = C_{s0} + \Delta C \quad (26)$$

$$C_{\text{out},n} = \frac{v_{n,\text{th1}} - v_{n,\text{th2}}}{V_{\text{ref}}}(C_T + C_s + C_p) \quad (27)$$

where it is assumed that the high-frequency input-referred noise of the comparator during ϕ_1 and ϕ_2 is uncorrelated. The main drawback of the SAR CDC compared with the SC CVC is apparent from (26), that is, the total sense capacitor has to be quantized, while C_{s0} carries no information and only ΔC is of interest. So, with

$$\text{SNR} = \frac{\Delta C^2}{\overline{C_{\text{out},n}{}^2}} \quad (28)$$

the SAR CDC must be implemented for an extended SNR range, SNR* defined as

$$\text{SNR}^* = C_{\text{out},s}^2/\overline{C_{\text{out},n}{}^2} = \left(\frac{C_{s0} + \Delta C}{\Delta C}\right)^2 \times \text{SNR}. \quad (29)$$

So, the resolution of the CDC must be increased by $\log_2(1 + C_{s0}/\Delta C)$ leading to a proportional increase in power consumption of the array. Total input-referred noise of the g_m-cell preamplifier with a dominant pole at ω_0 is

$$\overline{v_{n,\text{pre}}{}^2} = \frac{kT\gamma\alpha\omega_0}{g_m}. \quad (30)$$

The speed requirement on the preamplifier is stricter than that of the SC CVC, since here the output of the preamplifier has $T_s/2N$ s, compared with $T_s/2$ s of the SC CVC, to settle to within half-LSB error. So

$$\omega_0 \geq f_s N(N+1)\ln(2). \quad (31)$$

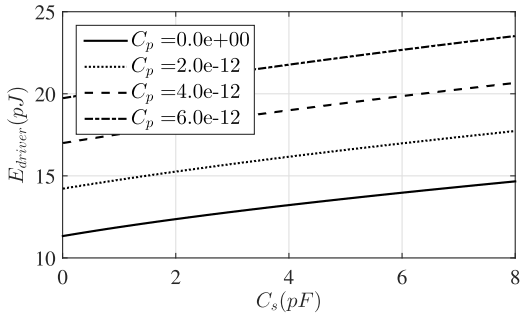

Fig. 9. Total switching energy consumption of the capacitive array.

In addition to (30), the switch noise sampled by the capacitive array at the time the reset switch opens, $kT/(C_T + C_s + C_p)$, also appears at the input of the comparator. The two noise components according to (27) result in

$$\overline{C_{\text{out},n}{}^2} = 2\left(\frac{kT}{C_T + C_s + C_p} + \frac{kT\gamma\alpha\omega_0}{g_m}\right) \times \left(\frac{C_T + C_s + C_p}{V_{\text{ref}}}\right)^2. \quad (32)$$

Using (28), (31), and (32), the relationship between SNR, g_m, and V_{ref} can be derived as

$$g_m = \frac{\alpha\gamma f_s N(N+1)\ln(2)}{\frac{2}{kT\text{SNR}}\left(\frac{\Delta C V_{\text{ref}}}{C_s + C_r + C_p + C_f}\right)^2 - \frac{1}{C_s + C_r + C_p + C_f}}. \quad (33)$$

The g_m expressed by (33) is N times larger than that of the SC CVC (20), and so in general, signal conditioning in the SAR CDC consumes more power than the SC CVC (this is at least partially offset by the fact that comparator preamplifiers generally do not require compensation and therefore have fewer transistors contributing to noise). This is a direct consequence of excess bandwidth requirement for digitization (31). Moreover, because the base capacitance C_{s0} also needs to be quantized in the SAR CDC, for the same ΔC, N of the SAR CDC is $\log_2(1 + C_{s0}/\Delta C)$ larger than N in the case of the SC CVC.

The switching energy (including CDS) of the capacitive array E_{driver} is a function of C_s, C_p, and V_{ref} (see the Appendix). To illustrate this, E_{driver} is plotted in Fig. 9. For small values of $C_p \approx 0$, E_{driver} is equal to that of the SC CVC half-bridge driver. It can also be noticed that E_{driver} is an increasing function of C_s (and C_p). So, as the worst case, we use the maximum value of C_s to estimate the power consumption of the capacitive array.

Using (21), (33), and (45), a set of noise-power optimization figures, similar to Fig. 7, can also be generated for the SAR CDC. Since the generation of an arbitrary voltage on the driver's side requires a dedicated dc/dc converter, we limit the discussion to the case where $V_{\text{ref}} = V_{\text{dd}}$. For design parameters listed in Table II, the minimum power consumption of the SC CVC and SAR CDC with respect to SNR is shown in Fig. 10(a). For the entire SNR range, the SC CVC is at least twice as more power efficient as the SAR CDC. In fact for SNR $>$ 60 dB, the SC CVC is about an order of magnitude

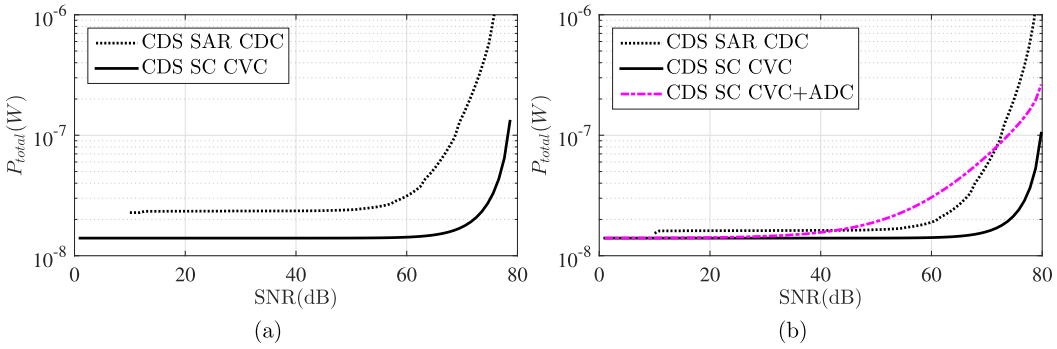

Fig. 10. Minimum power consumption comparison with $V_{\text{ref}} = V_{\text{dd}} = 1$ V, and the design parameters listed in Table II but different C_p values. (a) Minimum power consumption versus SNR for $C_p = 6$ pF. (b) Minimum power consumption versus SNR for $C_p = 1$ pF. The included ADC is assumed to have FOM = 10 fJ/conversion-step.

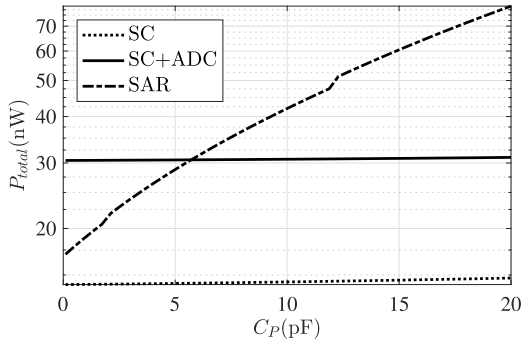

Fig. 11. Comparison of P_{total} of the SC CVC, SC CVC + ADC, and the SAR CDC as a function of C_P for 60 dB of SNR.

more power efficient than the SAR CDC. But, Fig. 10(a) does not account for required power consumption for digitization in the case of SC CVC. Therefore, the power consumption of an ADC, P_{ADC}, should also be included. Furthermore, it will be shown shortly that in this paper C_p can be as small as 1 pF. Fig. 10(b) reflects the effect of both P_{ADC} and $C_p = 1$ pF. The ADC is assumed to have a respectable figure of merit of 10fJ/conversion-step. Under these conditions, direct SAR CDC for 40 dB $<$ SNR $<$ 72 dB is found an optimal choice, if the parasitic interconnection capacitance can be kept small. However, for high-resolution digitization in presence of large parasitic capacitance, the cascade of SC CVC and an energy-efficient ADC is the optimal choice. Alternatively, for a given SNR, there exists a critical C_P which determines the optimal architecture. For instance, consider Fig. 11 which illustrates the total power consumption of different architectures for 60 dB of SNR as a function of C_P. For small $C_P < 5.78$ pF, the SAR CDC outperforms SC CVC + ADC, and for $C_P >$ 5.78 pF, the optimal choice would be the cascade of SC CVC and an energy-efficient ADC. Summarized in Table III is the qualitative comparison of the two interfaces under different conditions.

IV. Sensor Overview

Wire bonding external pressure transducers to the sensor interface IC is the traditional way of realizing a pressure-sensing system [40], [41]. This inevitably enforces a large

TABLE III
Qualitative Comparison of the SC CVC and the SAR CDC

	Output	SNR	C_p
SC CVC	Analog	–	–
SC CVC + ADC	Digital	Low-High	High
SAR CDC	Digital	Low-Medium	Low

parasitic interconnection capacitance C_p which needs to be either bypassed or tolerated by increasing the dynamic range of the interface to avoid interface saturation. As discussed in Section III, either of these solutions, however, tradesoff with the power consumption. Therefore, realizing an energy-efficient pressure-sensing system commands minimizing C_p.

Sensor-CMOS heterogeneous integration, first presented in [4], is the key solution to restrain C_p. A cross section of this integration type realized in Invensense MEMS-CMOS process [43] is shown in Fig. 1. This process offers eutectic bonding of a device wafer (including the membrane and the capping wafer) and a CMOS wafer. The top-metal layer in the CMOS wafer is designated to serve as the bottom plate of the sense capacitor. Thanks to the wafer-level bonding of the device and the CMOS wafers, C_p is limited to only the parasitic capacitance between top-metal layer of the CMOS and the ground silicon substrate. This capacitance can be estimated by knowing the dielectric constants and heights of the passivation layers sandwiched between the top-metal layer and the substrate. Designed for maximum sensor sensitivity, the dimensions of the bottom plate of the sense capacitor are 460×460 μm^2. In our process, there is a stack of 11 passivation layers resulting in a series interconnection of 11 capacitors whose values are 39.3 pF ($\times$5), 5.86 pF ($\times$5), and 8.81 pF ($\times$1). Thus, C_p is estimated 0.91 pF which is 55 times smaller than C_p reported in [40].

The membrane shown in Fig. 1 is an example of a square membrane with clamped edges. The plate behavior should be solved by finite-element techniques. Numerical methods, however, offer limited intuition as to how plate dimensions affect its deflection profile, unless computationally heavy parametric simulations are run. So, to gain insight into the

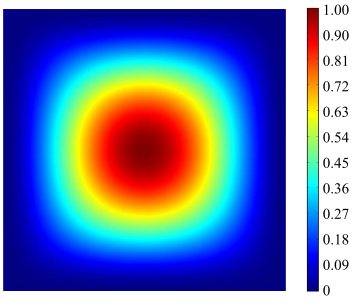

Fig. 12. Displacement profile of a clamped membrane under uniformly applied pressure. Displacement at each point is normalized to the maximum displacement.

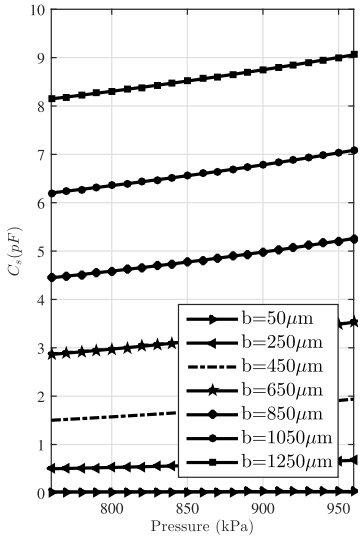

Fig. 13. Effect of bottom plate scaling on C_s, $a = 1.4$ mm.

plate mechanical behavior, Timoshenko's solution [44] for the maximum displacement of a thin clamped membrane under uniformly distributed applied pressure P deserves mention:

$$W_{\max} = 151 \times 10^{-3} \frac{1-\nu^2}{E} \frac{a^4}{t^3} P \tag{34}$$

where E and ν are Young's modulus and Poisson's ratio of the material of the plate, a and t are, respectively, the side length and the thickness of the plate. $W_{\max}$ occurs at the center of symmetry of the plate as shown in Fig. 12. To maximize deflection (sensitivity), the side length must be maximized and the thickness must be minimized. Since Invensense process is designed for inertial sensors, it utilizes a thick micrometers-scale membrane. This limits the maximum vertical displacement of the plate. The only design parameter of the plate is then a. The membrane side length can be calculated from (34) such that $W_{\max}$ is smaller than the gap height to avoid the collision of the membrane and the top-metal layer of the CMOS die. The side length calculated from (34) is then fine-tuned by numerical simulations, COMSOL Multiphysics, to account for other nonideal effects such as membrane thickness, the attachment of the capping wafer, and the stand-offs (MEMS-CMOS interconnection nodes). Our final simulated side length is 1.4 mm.

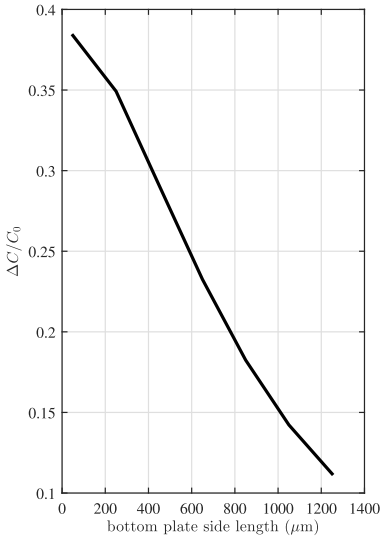

Fig. 14. Sensor sensitivity versus bottom plate side length, $a = 1.4$ mm.

As discussed in Section III, to decrease the switching energy consumption, it is favorable to minimize the base capacitance C_{s0} of the sensor. To accomplish this, sensor sensitivity $\Delta C/C_{s0}$ must be maximized. Note according to Fig. 12, the areas around the edges of the membrane experience little to no deflection and so contribute little to ΔC and most to C_{s0} if the bottom plate is center-aligned with the membrane and is a replica of it in size. Thus, the best practice is to scale down the bottom plate of C_s to concentrate the electric field in the center of the membrane (where maximum deflections happen) and to avoid contribution of the near-edge areas to C_{s0}. An example is shown in Fig. 13, where the bottom plate of the sense capacitor is swept from 50 to 1250 μm for a fixed membrane side length of 1.4 mm. The reduction of both C_{s0} and ΔC is clear for smaller bottom plate side lengths. But, as shown in Fig. 14, decreasing rate of C_{s0} is faster than that of ΔC, and the combined effects result in a better sensitivity. For the 400-μm side length, the sensitivity improves by almost 2.5 times. Further scaling the bottom plate side length results in an extremely small ΔC, in the order of tens of femtofarads, which severely limits the SNR and avoids medium-resolution quantization. So, we stop bottom plate down-scaling at 460 μm.

Membrane thickness and gap height both experience $\pm 10\%$ of process variation. Plotted in Fig. 15 is the deflection profiles of the cross section of the membrane on its axis of symmetry for the minimum and maximum pressures of interest. The displacement is normalized to the minimum gap height. The minimum and maximum C_s using the simulated profiles, shown in Fig. 16, are then obtained as 1.1 and 9.84 pF for, respectively, the worst membrane at 760 mmHg and the best membrane at 960 mmHg. The typical C_s is also simulated to vary from 1.56 to 2 pF under, respectively, 760 and 960 mmHg applied pressures. Thus, the SAR CDC full-scale range needs to exceed 9.84 pF to avoid saturation for 0–200 mmHg pressure range (and with $C_p = 0$). Smaller full-scale ranges, however, are also acceptable for ICP monitoring since the standard required range is 0–100 mmHg translating

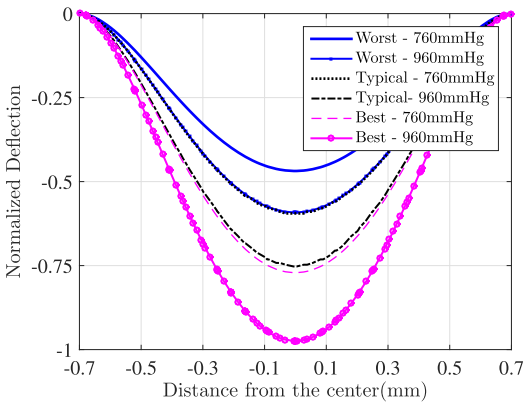

Fig. 15. Normalized (to the gap height) deflection profile of the membrane for different process corners.

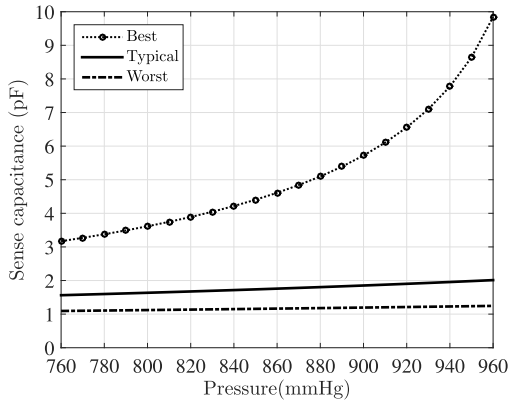

Fig. 16. Process corner simulation on the sense capacitance.

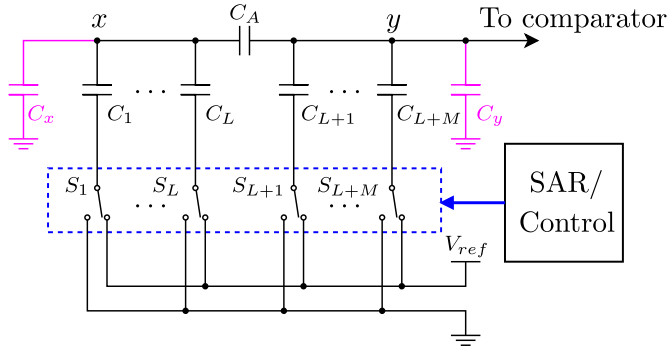

Fig. 17. Schematic of the split-capacitive array. C_x and C_y are the parasitic capacitors at each side of the array.

to maximally 4.6 pF full-scale range. Nonetheless, we choose 9.5 pF as the full-scale range of the CDC to account for nonzero (<4.6 pF) parasitic capacitance and a pressure range of 0–100 mmHg. In fact, since the total parasitic capacitance is ∼1.4 pF, the pressure range in the worst case would be extended to 0–150 mmHg.

V. CDS SAR CDC

The working principles of the proposed CDS SAR CDC used for this paper were discussed in Section III. Here, its implementation considerations and added features are discussed briefly.

TABLE IV
SAR CDC MODES OF OPERATION

Mode	Active Capacitors	C_0[fF]	C_Δ[fF]	C_{FS}[pF]
1	C_1–C_{12}	18.57	0.58	2.37
2	C_2–C_{13}	37.1	1.16	4.75
3	C_3–C_{14}	74.3	2.32	9.5

The minimum detectable pressure by the ICP monitoring system is 1 mmHg. For the least sensitive membrane at 760 mmHg, see Fig. 16, 1 mmHg translates to 0.75 fF (or 13.6-b of resolution with 9.5 pF full-scale range), whereas the smallest available metal–insulator–metal (MIM) capacitor in our process is 18.5 fF. Thus, to achieve the desired resolution, split-capacitive array [45] is deployed. An N-bit binary-weighted split-capacitive array with the attenuating capacitor C_A is shown in Fig. 17 where

$$C_i = \begin{cases} 2^{i-1}C_0, & 1 \le i \le L \\ 2^{i-L-1}C_0, & L+1 \le i \le L+M \\ \dfrac{2^L}{2^L-1}C_0, & i = A \end{cases}$$

and L is the number of branches in the LSB side of the array, $M = N - L$ is the number of MSB-side branches, and C_0 is the unit capacitor of the array. Assuming that C_0 is chosen the minimum available MIM capacitor $C_{\text{MIM,min}} = 18.5$ fF, to achieve a resolution better than $C_\Delta = 0.75$ fF, the number of LSB-side branches needs to be

$$L = \left\lceil \log_2 \frac{C_{\text{MIM,min}}}{C_\Delta} \right\rceil = 5. \tag{35}$$

So, with 14 b of resolution, the split-capacitive array of Fig. 17 with five LSB-side branches and C_0 of 18.5 fF is equivalent to a 14-b normal binary-weighted capacitive array with $C_0 = C_\Delta$ of 0.57 fF.

Note that, in Fig. 16, both the sensitivity and the base capacitance of C_s increase from the worst to the best membrane. This means that the worst membrane needs a smaller full-scale range C_{FS} and a finer C_Δ, but the best membrane needs a larger C_{FS} and C_Δ. As an example, consider a typical sense capacitance which ranges from 1.5 to 2 pF. Having a maximum full-scale range of 9.5 pF for resolving the typical sense capacitor is costly in terms of capacitive array switching power, because in this case in every conversion, the two MSB capacitors are charged wastefully. So, to further adapt the CDC to the sense capacitor, programmability is incorporated to its full-scale range and resolution C_Δ. The SAR CDC has three modes of operation. For all the three modes, the number of bits is kept constant, but the full-scale range and the LSB capacitance C_Δ are doubled. In all the three modes, only 12 capacitors (out of 14) take part in the SAR process and the other two capacitors float using tristate switches. The full-scale range and resolution for each mode is summarized in Table IV. Thus, according to the sense capacitor regardless of process variations, the best full-scale range and C_Δ can be selected.

Fig. 18 shows the circuit diagram of the programmable SAR CDC. The positive terminal of the comparator is pulled

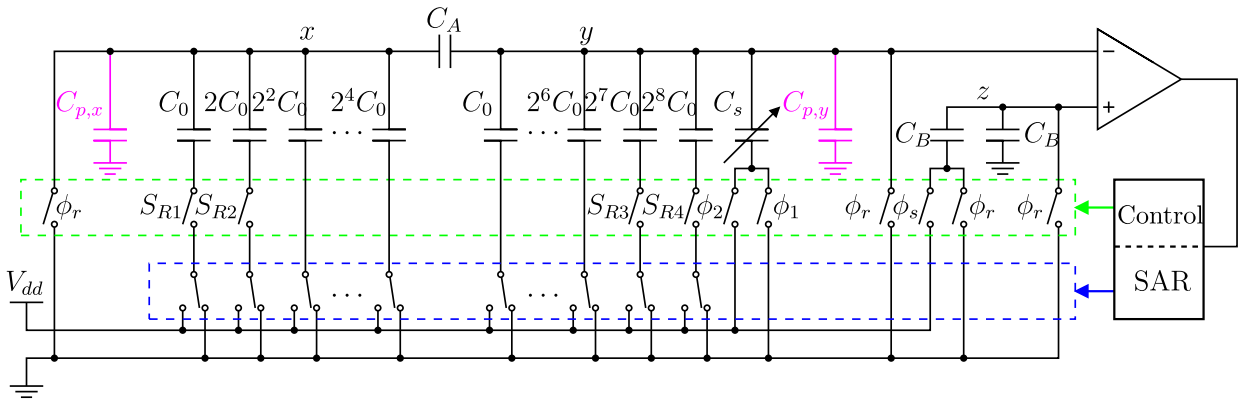

Fig. 18. SAR CDC circuit diagram. Four tristate switches are used for full-scale range selection, and T-switches are used for minimizing leakage from the floating nodes x, y, and z.

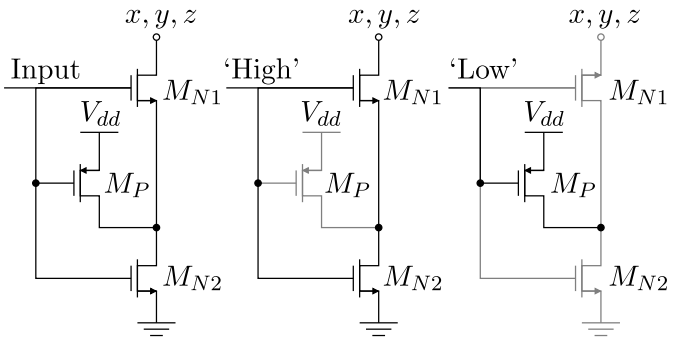

Fig. 19. T-type reset switch.

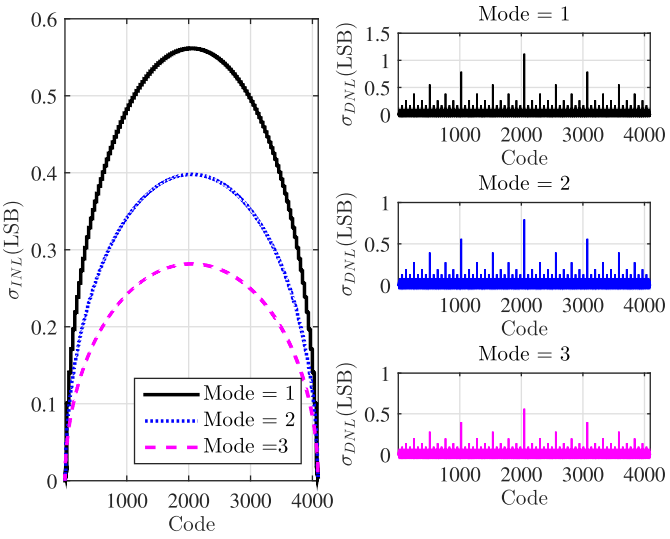

Fig. 20. Calculated σ_{INL} and σ_{DNL} of the capacitive array for different settings of Table IV.

to $V_{\text{dd}}/2$ at the beginning of each conversion period by the help of two identical capacitors C_B. To minimize capacitance asymmetry at the input terminals of the comparator, these bias capacitors should be half of the total capacitance of the array, $C_B = C_T/2$. To avoid charge accumulation at the positive terminal of the comparator V_z, at the end of each conversion period, C_Bs are discharged by a reset switch. The charge leakage through this reset switch during conversion periods, however, causes the reference voltage to drift away from $V_{\text{dd}}/2$. If an NFET is used as the reset switch, V_z decreases at a rate of 0.88 V/s, limiting the sampling rate to 7.2 kHz for 12 b of resolution. Thus, this reset switch is realized by a three-transistor T-type switch shown in Fig. 19. When the reset signal is high, M_P is OFF, and the two NFETs normally discharge the bias capacitors to ground. When the reset signal toggles to low, the NFETs turn off and M_P pulls the drain of M_{N2} high. As a result, the source and drain of M_{N1} swap roles and it experiences a negative gate–source voltage during the conversion period. This negative V_{gs} significantly enhances the OFF-resistance of the switch. Simulation results show that using this T-switch decreases the voltage V_z drift rate to 0.29 mV/s allowing sampling rates down to 3 Hz. Although the same T-switches are used to implement the reset switches of the array at nodes x and y, the leakage charge through tristate switches serves as the bottleneck for the sampling rate constricting it to 650 Hz.

TABLE V

PARASITIC CAPACITANCE IN FEMTOFARAD ACROSS THE CAPACITORS OF THE ARRAY WITH AND WITHOUT THE GROUND PLANE

	WOG	WG		WOG	WG
$\mathbf{C_1}$	1.9	1.2	$\mathbf{C_2}$	2.4	2.1
$\mathbf{C_3}$	4.7	4.1	$\mathbf{C_4}$	9.2	8.2
$\mathbf{C_5}$	17.6	16.5	$\mathbf{C_6}$	1.7	1
$\mathbf{C_7}$	3.2	2.1	$\mathbf{C_8}$	5.9	4.84
$\mathbf{C_9}$	9.4	8.8	$\mathbf{C_{10}}$	19.5	18.2
$\mathbf{C_{11}}$	39	36.3	$\mathbf{C_{12}}$	78.9	73.7
$\mathbf{C_{13}}$	157.5	147.8	$\mathbf{C_{14}}$	313.9	295.1
$\mathbf{C_{p,x}}$	11.7	55.5	$\mathbf{C_{p,y}}$	131.3	728.2
$\mathbf{C_A}$	5.6	1.7	—	—	—

The nonlinearity of the binary-weighted split array was also considered in the design. The derivation of $\sigma_{\text{INL}}/\sigma_{\text{DNL}}$ is out of the scope of this paper, and here, we only report on the

final expressions and the results. If the binary representation of the input code is $\mathbf{D} = [D_N, D_{N-1}, \ldots, D_1]$, ${\sigma_{\text{INL}}}^2[D]$ can be expressed by

$$
\begin{aligned}
&{\sigma_{\text{INL}}}^2[D] \\
&= \left(\frac{\sigma_0}{C_0}\right)^2 \times \left(2^{2L} \sum_{i=L+1}^{L+M} (2^{i-L-1}(D_i - B[D])^2) \right. \\
&\qquad \left. + \sum_{i=2}^{L} 2^{i-1}(D_i - B[D])^2 \right) + (D_1 - 1)^2)
\end{aligned} \tag{36}
$$

where $B[D] = (D-1)/(2^N - 2)$, and σ_0 is the standard deviation of the unit capacitance error. In our 0.18-μm process $(\sigma_0/C_0) \approx ((6 \times 10^{-10})/\sqrt{C_0})$. The INL and the DNL of the array for the three modes of operation of the CDC is shown in Fig. 20 confirming that the CDC in the worst case (with the smallest C_0) should maintain better than 0.6LSB of INL.

The capacitive array in presence of parasitic capacitance suffers further systematic nonlinearity. This is because of nonbinary-weighted parasitic capacitance (due to routing) across capacitors of the array. Table V summarizes postlayout parasitic extraction of various capacitors of the array. Including the parasitic capacitors, the array exhibits a large systematic INL as shown in Fig. 21 (black solid lines). To remedy this, an M4 ground plane was placed to shield the top (M5) and bottom (M1/M2) plate routing traces. The ground plane makes the parasitic capacitance across the array capacitors more binary weighted (see Table V). This layout technique also decreased the parasitic capacitance across C_A by three times. The ground plane increases $C_{p,y}$ by 5.5 times to 730 fF, but this is a minor effect because this C_P is still an order of magnitude smaller than the full-scale range of the CDC. Nevertheless, the overall effect of the ground plane on the systematic INL is also shown in Fig. 21 which shows more than two times of improvement.

VI. Measurement Results

The pressure-sensing system was fabricated in 0.18-μm Invensense MEMS process. For all measurements, the CDC works in the third mode where it has the largest full-scale range and its dynamic power consumption is maximum. In addition to the pressure-sensing core, the chip contains bias generation, power on reset circuitry, and a 40-kHz sawtooth oscillator for clock generation. The SAR comparator is of regenerative type [46]. To prevent any postprocessing, the upper cavity was extended to the MEMS device dicing edge such that a 200-μm-wide inlet was automatically formed when the device wafer was diced, as shown in Fig. 22.

A custom-designed pressure chamber was used to characterize the sensor. The measurement environment included the chamber, a pneumatic pressure pump (Additel 901), and a precision pressure gauge (Fluke 700GA4). The chip and the gauge were enclosed in the chamber. During measurement, pressure was swept from 540 to 1060 mmHg at 10 mmHg/step. Shown in Fig. 23 is the obtained capacitance–pressure curve of the sensor.

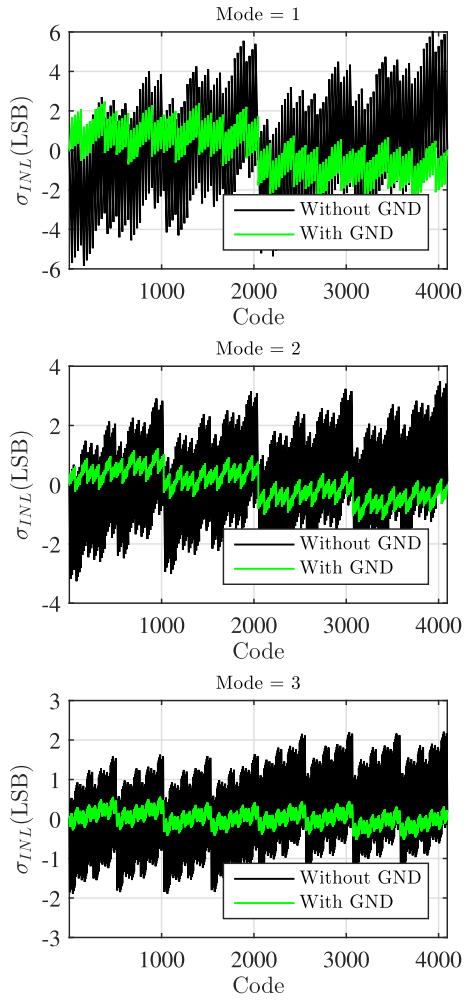

Fig. 21. σ_{INL} after parasitic extraction with and without the ground plane.

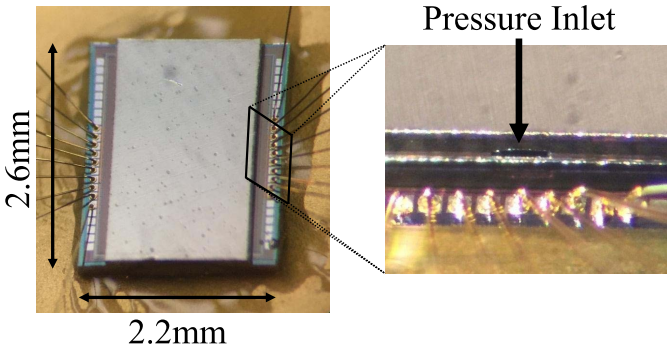

Fig. 22. Chip photograph and the pressure channel to the upper cavity.

There exists a mismatch between the measured capacitance and the finite-element simulation presented earlier. More specifically, the measured base capacitance C_{s0} is larger than expected. High linearity of the sensor (0.2% of nonlinearity) at this large base capacitance hints at the possibility that the sensor operates in a touch-mode rather than the normal mode of operation. Careful investigation of the

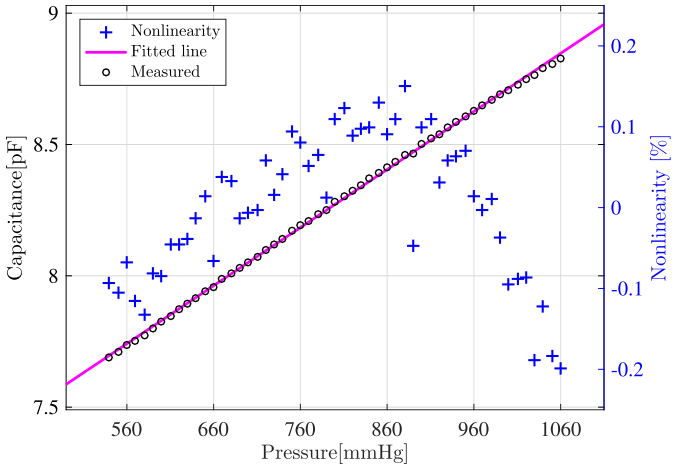

Fig. 23. Capacitance versus pressure curve.

system revealed a layout error is responsible for the observed mismatch. No pad opening window was placed over the top-metal layer (the bottom plate of the sense capacitor), and consequently two (SiO_2 and Si_3N_4) passivation layers were left between the two plates of the sense capacitor decreasing its gap height by 40%. Finite-element simulations confirm with the reduced gap size that the sense capacitor indeed operates in the touch-mode. The mismatch between the simulated and measured C_s would be eliminated, if the top-metal layer had been properly exposed. Nonetheless, the current touch-mode sensor covers the entire pressure range required for ICP monitoring.

To confirm our heterogeneous sensor-CMOS integration results in minimal C_p, parasitic capacitance is estimated by the help of the measured sensor characteristic shown in Fig. 23. Note that for any applied pressure P, the interface outputs $C_{\phi 1}$ and $C_{\phi 2}$. Denoting $C_A = C_{\phi 1} + C_{\phi 2}$, (23) and (24) result in

$$C_A(p) = C_T + C_P - 2\frac{V_{\rm OS}}{V_{\rm ref}}(C_T + C_P + C_s(P)) \quad (37)$$

where the only unknown variables are $V_{\rm OS}$ and C_p. So, for two applied pressures, e.g., 540 and 640 mmHg, (37) can be solved for C_p and $V_{\rm OS}$ as 1.45 pF and 21 mV, respectively. According to Table V, 728 fF of this C_p is due to the routing traces, and thus, the current integration method gives rise to only 722 fF of C_p.

The sensor sensitivity is measured 2.2 fF/mmHg with 0.2% sensor and CDC *combined* nonlinearity. The total power consumption of the converter core is just below 50 nW at 650 S/s (Fig. 24). Temperature drift of the system is shown in Fig. 25 where the readout pressure error is negligible for temperatures below 37 °C. It, however, increases for temperatures above 37 °C by a rate of 1.8 mmHg/°C. Responsible for the readout error for temperatures above 40 °C is the decreased (sampling) frequency of the oscillator which in turn results in higher leakage current through tristate switches. Allan deviation of the sensor is also reported in Fig. 26, suggesting that a noise floor of 2.16 mmHg (4.75 fF) is achieved when sampling at 60 Hz. Providing that the

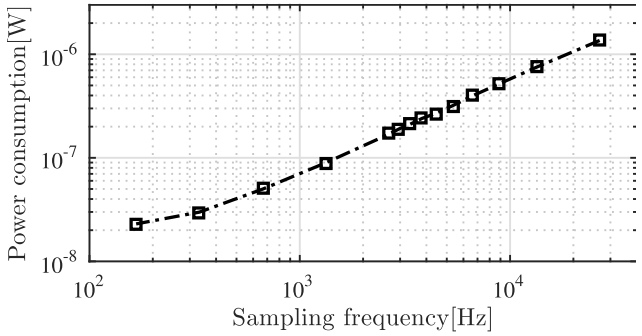

Fig. 24. Power consumption versus sampling frequency.

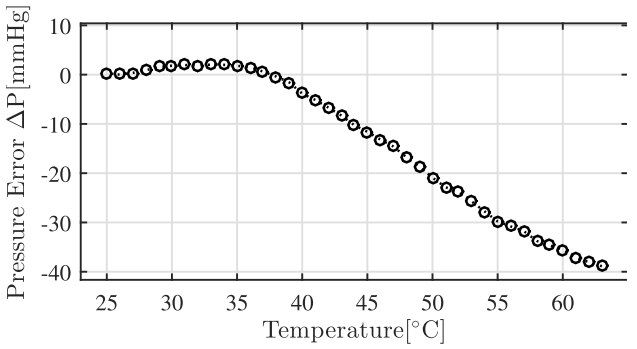

Fig. 25. Pressure drift from its nominal value (atmospheric pressure at room temperature) versus temperature change.

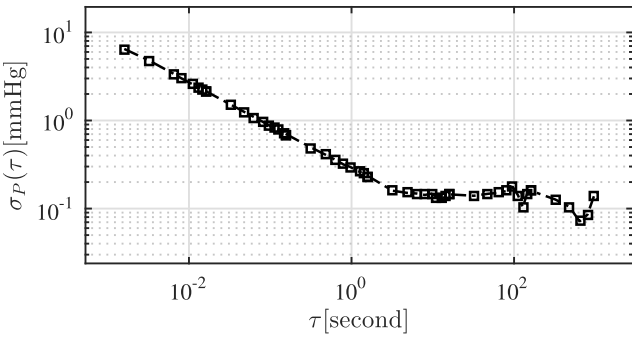

Fig. 26. Allan deviation.

input range of the SAR CDC is 9.5 pF, its SNR and FOM based on the definitions given in [30] [SNR = 20 log ((Cap. input range/$2\sqrt{2}$/Cap. resolution)], FOM = (Power/($f_s \times 2^{(\rm SNR-1.76)/6.02}$)) are, respectively, 57 dB and 3.9 pJ/conversion-step. These performance metrics are comparable to those of recent state-of-the-art pressure-sensing systems as summarized in Table VI. The power consumption of the system and the obtained pressure resolution (2.16 mmHg) make it suitable for ICP monitoring.

VII. Conclusion

A millimeter-scale pressure-to-digital microsystem targeting ICP monitoring was presented. The device measures only 0.4 mm in height thin enough to be implanted in the subarachnoid space. Through careful circuit analysis, energy efficiency

TABLE VI
PERFORMANCE SUMMARY AND COMPARISON OF RECENTLY PUBLISHED CAPACITIVE SENSING SYSTEMS

	[29]	[25]	[31]	[30]	[37]	[41]	**This work**
Sensor type	–	–	–	External	Integrated	External	**Integrated**
CDC Architecture	ΣΔ	ΣΔ	IDCD	Slope	ΣΔ	SAR	**SAR**
Technology	0.18μm	0.16μm	0.04μm	0.18μm	0.8μm	0.18μm	**0.18μm**
Fabrication post-processing	–	–	–	Yes	Yes	Yes	**No**
Input Range(pF)	0–24	0.54–1.06	0.7–10000	5.3–30.7	2.53	2.5–75.3	**9.5**
Power	33.7μW	10.3μW	1.84μW	110nW	1.4mW	160nW	**130nW**
Sensitivity(fF/mmHg)	–	–	–	17.5	1.35	27	**2.2**
Sampling freq.	4.29kHz	1.25kHz	52.6kHz	156Hz	100kHz	250Hz	**60Hz**
Resolution	0.15fF	70aF	12.3fF	8.7fF	0.17fF	6fF	**4.75fF**
SNR(dB)	94.7	68.4	49.7	44.2	74	55.4	**57**
FOM(pJ/Conv.-step)	0.18	3.8	0.14	5.3	899	1.3	**3.9**
Supply	1.4V	1.2V	0.45–1V	1.2-4V	3.5V	0.9–1.2V	**1V**
System Volume	–	–	–	6.27mm^3	1.52mm^3	–	**2.29mm^3**

of the system was found correlated with the parasitic interconnection capacitance whose minimization (down to 720 fF) was performed by heterogeneous sensor-interface integration. Measurement results of the fabricated chip showed comparable performance to the state-of-the-art systems without any fabrication postprocessing. The measured pressure range, resolution, and sampling rate meet the requirement for ICP measurements.

APPENDIX

To calculate the total switching energy of the N-bit SAR CDC shown in Fig. 8, the sum of packets of charge drawn from V_{ref} must be determined during the SAR bit-cycling process for both the phases ϕ_1 and ϕ_2. During the reset phase, all the capacitors are discharged to ground. In ϕ_1, the sense capacitor C_s and the MSB capacitor of the array C_1 are switched to V_{ref}. This results in the voltage of the floating node v_x to jump to $v_{x,\phi1}[1] = ((C_s + C_1)/(C_T + C_s + C_p))V_{\text{ref}}$. So, the amount of charge required to charge C_s and C_1 from 0 to $V_{\text{ref}} - v_{x,\phi1}[1]$ is, respectively

$$Q_{s,\phi1}[1] = C_s(V_{\text{ref}} - v_{x,\phi1}[1]) \tag{38}$$
$$Q_{a,\phi1}[1] = C_1(V_{\text{ref}} - v_{x,\phi1}[1]). \tag{39}$$

At the end of ϕ_1 according to (23), the digital representation $\mathbf{D}_{\phi\mathbf{1}}$ of $C_{\phi1}$ is available. $\mathbf{D}_{\phi\mathbf{1}}$ is an array of binary values $\mathbf{D}_{\phi\mathbf{1}} = [D_{\phi1}(1), D_{\phi1}(2), \cdots D_{\phi1}(N)]$, where $D_{\phi1}(i)$ is the output of the comparator after the ith comparison. For known C_s and C_p, $\mathbf{D}_{\phi\mathbf{1}}$ can be calculated. Then, v_x after the ith switching step during ϕ_1 can be derived as

$$v_{x,\phi1}[i] = \frac{C_s + C_i + \sum_{k=1}^{i-1} D_{\phi1}(k)C_k}{C_T + C_s + C_p} V_{\text{ref}}. \tag{40}$$

Consequently, (38) and (39) for the ith ($2 \le i \le N$) step are given by

$$Q_{s,\phi1}[i] = C_s(v_{x,\phi1}[i-1] - v_{x,\phi1}[i]) \tag{41}$$
$$Q_{a,\phi1}[i] = \left(C_i + \sum_{k=1}^{i-1} C_k D_{\phi1}(k)\right) \times (v_{x,\phi1}[i-1] - v_{x,\phi1}[i]) + C_i V_{\text{ref}}. \tag{42}$$

Using (38)–(42), the total charge drawn from V_{ref} during ϕ_1 can be expressed by $Q_{\phi1} = \sum_{i=1}^{N}(Q_{s,\phi1}[i] + Q_{a,\phi1}[i])$.

A similar analysis can be applied to derive $Q_{\phi2}$. Since C_s is grounded in this phase $Q_{s,\phi2} = 0$, and only $Q_{a,\phi2}$ needs to be considered. The voltage v_x after the MSB capacitor of the array C_1 is switched to V_{ref} is given by

$$v_{x,\phi2}[1] = \frac{C_1}{C_T + C_s + C_p} V_{\text{ref}} \tag{43}$$

which translates to a transfer of charge equal to $Q_{a,\phi2}[1] = C_1(V_{\text{ref}} - v_{x,\phi1}[1])$ from V_{ref} to C_1. For $2 \le i \le N$, (43) takes the form of

$$v_{x,\phi2}[i] = \frac{C_s + C_i + \sum_{k=1}^{i-1} D_{\phi2}(k)C_k}{C_T + C_s + C_p} V_{\text{ref}} \tag{44}$$

where $D_{\phi2}(i)$ is the ith MSB-bit of the output code. By using (44), the charge drawn from V_{ref} at the ith ($2 \le i \le N$) SAR step can be expressed by $Q_{a,\phi2}[i] = (C_i + \sum_{k=1}^{i-1} C_k D_{\phi2}(k))(v_{x,\phi2}[i-1] - v_{x,\phi2}[i]) + C_i V_{\text{ref}}$, and the total charge transfer during ϕ_2 will be given by $Q_{\phi2} = \sum_{i=1}^{N} Q_{a,\phi2}[i]$. Finally, the total switching energy consumption associated with the capacitive array of the CDS SAR CDC is given by

$$E_{\text{driver}} = (Q_{\phi1} + Q_{\phi2})V_{\text{ref}}. \tag{45}$$

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