A 0.013 mm^2, 5 μW, DC-Coupled Neural Signal Acquisition IC With 0.5 V Supply

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***Abstract*—We present an area-efficient neural signal-acquisition system that uses a digitally intensive architecture to reduce system area and enable operation from a 0.5 V supply. The architecture replaces ac coupling capacitors and analog filters with a dual mixed-signal servo loop, which allows simultaneous digitization of the action and local field potentials. A noise-efficient DAC topology and an compact, boxcar sampling ADC are used to cancel input offset and prevent noise folding while enabling "per-pixel" digitization, alleviating system-level complexity. Implemented in a 65 nm CMOS process, the prototype occupies 0.013 mm^2 while consuming 5 μW and achieving 4.9 μVrms of input-referred noise in a 10 kHz bandwidth.**

***Index Terms*—Area-efficient, biomedical, boxcar sampling, brain–machine interface, CMOS, low noise, low power, medical implants, mixed-signal architecture, offset cancellation, sensor interface.**

I. Introduction

RECENTLY, information technology's impact on the healthcare system has begun to accelerate. Advancing our ability to interface electrical systems with biological environments will enable patients to be monitored and receive treatment at home, and in the long term, have electronic devices chronically implanted. In particular, recent research in brain–machine interfaces has shown success in decoding electronic signals from the motor cortex of the brain to control artificial limbs in both primates and humans, providing hope for patients with spinal cord injuries, Parkinson's disease, and other debilitating neurological conditions [1], [2]. Current neural interfaces are large, wired and require open-skull operation; future minimally invasive, fully implantable interfaces with signal processing and wireless capabilities will enable prosthetics, disease control, and completely new user–computer interfaces.

Fig. 1 shows the components required for a fully implantable wireless neural recording system. Batteryless operation requires wireless power coupling, while wireless data transmission eliminates wires, allowing the surgeon to close the surgical site, thus restoring mobility and lessening the risk of infection. A mixed-signal front-end is required to digitize the signals from each electrode. To record from multiple sites simultaneously, one front-end is required per active electrode, thus the implanted chip may have hundreds of arrayed data acquisition channels, which dominate the chip area and power in current implementations [3], [4]. Future electrode arrays with greater number and density of recording sites will only increase the power and area constraints placed on these front-ends. In order to address these challenges, this paper describes a complete neural signal acquisition channel in 65 nm CMOS and operating at a 0.5 V supply that obtains state-of-the-art performance in a silicon area over three times smaller than the smallest neural amplifier previously reported [3]. A compact solution is obtained by using a system architecture tailored to an advanced process that avoids on-chip passives and takes advantage of high-density logic and aggressive process voltage scaling to reduce power and area.

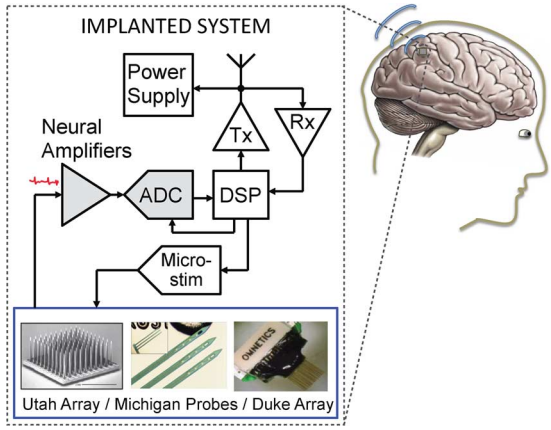

Fig. 1. Block diagram of an integrated circuit for an implantable neural recording system. The inset at the bottom of figure shows examples of commonly used electrodes.

This paper is organized as follows. In Section II, we discuss the requirements and challenges of performing neural signal acquisition with minimal power dissipation and area. Section II further discusses the state of the art in neural recording and the proposed front-end architecture of this work. Section III details the design of the individual circuit blocks, emphasizing noise/power efficiency, and low area occupation. Measurement results, including *in vivo* cortical recordings taken from a live rodent, are described in Section IV. Finally, conclusions will be given in Section V.

II. Neural Signal Acquisition

The key challenge in the design of a neural signal acquisition chain is in separating the μV-level desired signal from large offsets and low-frequency disturbances. In this case, a dc offset as

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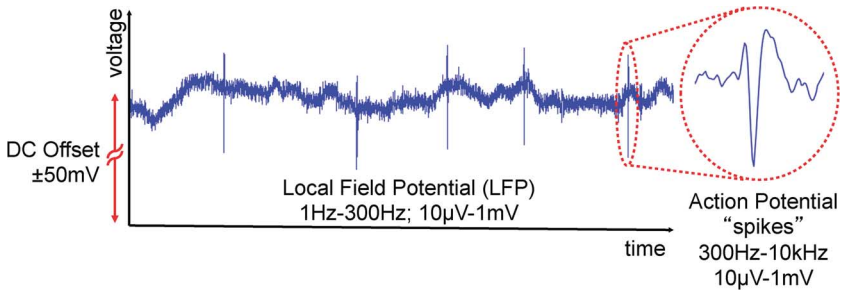

Fig. 2. Representative neural signal at the electrode/circuit interface.

large as 50 mV is associated with the electrodes. Superimposed on the offset, the information-bearing signal is composed of a slowly varying (<300 Hz) Local Field Potential (LFP), representing a spatial average of neural activity in the neighborhood of the electrode, and of higher frequency (300 Hz–10 kHz) Action Potential or "Spike" events, associated with the firing of individual neurons in the immediate proximity of the electrode as shown in Fig. 2.

Both LFPs and Spikes are relevant in prosthetics and neuroscience [5]; it is therefore optimal to digitize both signals simultaneously. The relative magnitude of these signals depends on the location of the recording electrode and its proximity to the neurons. In a worst-case condition, spikes with amplitudes of the order of tens of microvolts can appear simultaneously with LFPs with amplitudes of 1 mV. Assuming a minimum signal-to-thermal-noise ratio requirement of 10 dB for Spike digitization, input-referred noise of the order of 5 μVrms is required. The total dynamic range required by the acquisition chain is approximately 50 dB after offset removal, and >80 dB including the offset. Therefore, if all signals were digitized together using a single ADC, resolution in excess of 14 bits would be required. This requirement makes signal conditioning prior to A-to-D conversion necessary in order to obtain a compact and power-efficient solution.

State-of-the-art neural signal acquisition systems [3], [4], [6], [7] typically employ an acquisition chain such as the one shown in Fig. 3(a), consisting of a low-noise amplifier (LNA), a bandpass filter to filter either the spike or LFP bands, an analog sample-and-hold, and a multiplexer which serializes multiple channels into a single high-sample-rate ADC. These designs have relied heavily on analog techniques to implement the LNA and bandpass filter by using AC-coupled instrumentation amplifiers with capacitive feedback followed by analog filtering [Fig. 3(b)]. The input ac-coupling capacitors ($C_{\rm IN}$) simultaneously serve the purpose of blocking leakage to the electrodes, and rejecting the large and unknown electrode offset and common mode. The values of capacitance required by $C_{\rm IN}$ and C_F are determined by the time constants required for offset and LFP separation as well by the maximum resistor values that can be implemented. For typical values of a 1-Hz high-pass pole, $R_{\rm DC} = 100$ GΩ and $C_{\rm IN}/C_F = 100$, we find $C_F = 0.25$ pF and $C_{\rm IN} = 25$ pF. In a standard process, even if linear capacitors with density of 2 fF/μm^2 were available, the area occupied by $C_{\rm IN}$ alone would be 0.025 mm^2. A literature survey [8] confirms that it is difficult to scale the area of a complete neural acquisition chain utilizing ac coupling below 0.04 mm^2.

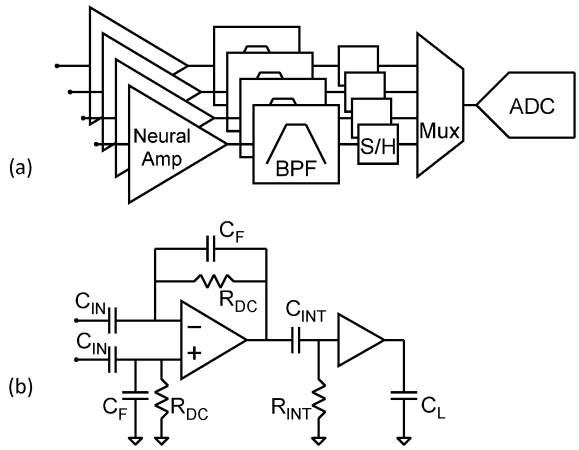

Fig. 3. (a) State-of-the-art multichannel signal acqusition chain and (b) neural amplifier and bandpass filter.

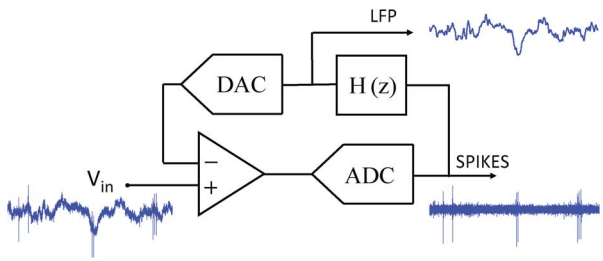

Fig. 4. Mixed-signal feedback architecture.

A. *Front-End Architecture Selection*

In order to scale the die area occupied by the signal acquisition chain below this mark and to enable simultaneous LFP and spike digitization, we employ the alternative architecture shown in Fig. 4 [9]. The ac coupling capacitors are removed, and the offset is mitigated using a mixed-signal feedback loop. The forward path is composed of a broadband instrumentation amplifier that is dc-coupled to the electrodes and an ADC, while the feedback path, comprised of a DAC and a digital low-pass filter $H(z)$, realizes a servo-loop that suppresses the offset and the LFP. Feedback forces the output of the digital low-pass filter to reproduce the sum of the low-frequency components, reducing the dynamic range requirement of the instrumentation amplifier

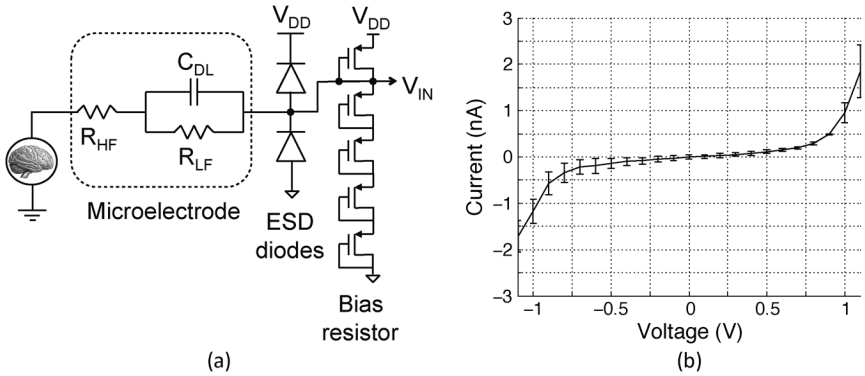

Fig. 5. (a) Microelectrode small-signal model and IC interface. (b) Average and standard deviation I–V curves of "Utah-style" microelectrodes from a single array. The measurement is made differentially across two electrodes.

and ADC cascade. Therefore, the ADC outputs a digitized version of the "high-frequency" Spike band. In addition, the output of the digital filter provides a digitized version of the low-frequency components and becomes the LFP output. Both LFP and Spike bands are thus digitized simultaneously using the same hardware. The large time constants necessary to effectively separate the two components are realized in a compact footprint by $H(z)$ using digital gates.

When realized in a 65-nm process, the architecture in Fig. 4 has several advantages over traditional solutions such as low area, programmability and "per-pixel" digitization, which replace the complicated routing of analog signals at the top level. The efficient realization of the architecture presents a few challenges that are discussed in detail in the following subsections.

B. Electrode Interface and Safety

Since the integrated circuit makes direct contact with the electrodes it is important to make sure that safe current levels are maintained in both normal operation and when there is an electrostatic discharge (ESD) failure. At the same time, the on-chip common-mode voltage must be stabilized. A string of diode-connected subthreshold MOSFETs is used to stabilize the dc common mode voltage in a method similar to [10] to 4/5 $V_{\rm DD}$ or 400 mV (Fig. 5(a)). The small-signal dc resistance of the on-chip bias network is approximately 1 GΩ. Constraints on accuracy and matching of the resistors are relaxed since the offset is cancelled and the refresh rate can be programmed to cancel drift in electrode offset and dc characteristics.

Ideally the circuit can interface with a variety of microelectrodes such as those shown in Fig. 1. A simplified small-signal model of an electrode is shown in Fig. 5(a). The dc resistance of the electrodes $R_{\rm LF}$ given by the equilibrium exchange current is very high; for example, a platinum microelectrode with an area of 1000 μm^2 has $>$ 30 GΩ of dc resistance [11]. Fig. 5(b) confirms that Utah-style microelectrodes with platinum tips have a resistance $>$ 30 GΩ in their linear range. In parallel to this resistor, a capacitor $C_{\rm DL}$ (formed by the electrical double layer at the metal-tissue interface) dominates the impedance in the signal band. A more accurate model for $C_{\rm DL}$ is a constant phase element whose capacitance changes with frequency and is on the order of 1–3 nF at 1 Hz. The chosen 1 GΩ bias network impedance stabilizes the dc operating point while setting (together with $C_{\rm DL}$) a high-pass filter pole below the 1 Hz signal bandwidth. As a result, thermal noise generated by the bias network in either the LFP or the spike band is shunted by $C_{\rm DL}$ and does not impact the system noise floor.

Fig. 5(b) shows measured I–V curves for the current between two electrodes of a Utah-style polysilicon microelectrode array from Blackrock Microsystems measured in phosphate buffered saline (PBS). In the event of an ESD failure, a worst-case voltage equal to the on-chip power supply voltage of 0.5 V is applied across the electrodes and a worst-case current of approximately 200 pA results, which is well within safe levels of operation [12]. In comparison, an IC with a $V_{DD} = 1$ V would suffer currents ten times larger due to the nonlinearity of the I–V relation. Bubbles in the PBS/electrode interface are visually observed at approximately $\Delta V \geq 3.8$ V$_{\rm DC}$.

C. Gain and Offset Correction Range Allocation

Open-circuit potential measurements of the electrodes show that offsets can be of the order of hundreds of mV. Because of the large value of $R_{\rm LF}$, even if there is an open-circuit potential of 1 V, the offset seen at the chip input will be attenuated by the on-chip resistor to 30 mV, and the dc current flowing through those electrodes will be 15 pA, which is well below electrolysis-inducing current levels. In this implementation, an offset range of $\pm$50 mV was chosen; however, this range could be extended, as will be discussed in Section IV. For typical values of offset (up to $\pm$50 mV) and assuming a maximum input-referred noise floor of 5 μVrms, the DAC in Fig. 4 requires a resolution of 16 bits to suppress quantization noise well below the thermal noise floor. To mitigate the DAC resolution requirements, the offset and LFP cancellation is split into a dual-loop architecture that uses a coarse-fine approach, as shown in Fig. 6. First, a 7-bit DAC performs coarse offset cancellation, reducing the total offset processed by the acquisition chain from $+/-50$ down to 1 mV. The noise and common-mode rejection requirements of this DAC are critical and require the use of special circuit techniques described in the next section. The second, fine loop has a DAC resolution of 9 bits, which is necessary to suppress the residual offset as well as the LFP signals without degrading the SNDR in the spike band. The time scales of the

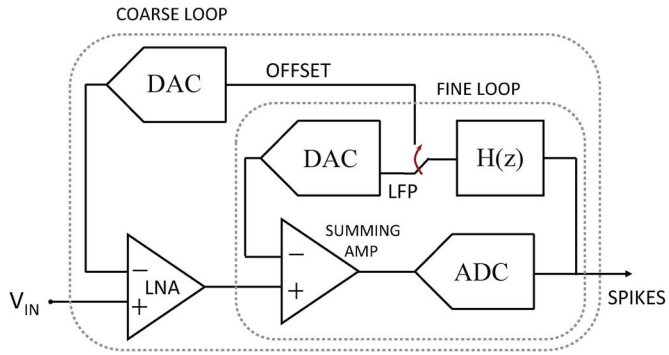

Fig. 6. Split dual-loop architecture: coarse loop cancels offset, while fine loop cancels LFP with residual offset.

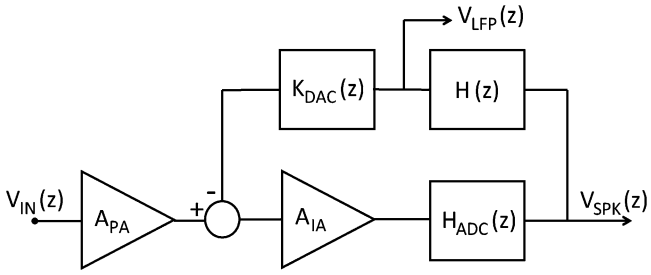

Fig. 7. Feedback block diagram representation of neural signal acquisition chain.

coarse and the fine offset loops are separated: coarse offset cancellation is performed at slow rates (programmable between 0 and 1 Hz) using a binary search, while the fine loop is closed through a linear filter $H(z)$ and has bandwidth comparable to the LFP.

D. Noise Folding

Since the forward path is broadband compared with the signal bandwidth, sampling its output without an anti-aliasing filter before digitization would lead to out-of-band noise aliasing, reducing power efficiency. For example, a 1 MHz overall forward path bandwidth sampled at 20 kS/s would incur a 50× noise folding penalty. To prevent this penalty, and to avoid the added area of having an explicit analog filter for anti-aliasing, we chose to use a boxcar sampling ADC [13] running at the 20 kS/s Nyquist rate.

E. Filter Design

A high-pass transfer function $(G_{\rm SPK})$ is required in order to remove the LFP and residual offset from the spike output. The use of feedback introduces a tradeoff between the choice of loop filter and loop stability. With reference to the block diagram in Fig. 7, defining $H(z)$ as the transfer function of the digital low-pass filter in the feedback path, the transfer function from the electrodes to the ADC output is

$$G_{\rm SPK}(z)=\frac{V_{\rm SPK}(z)}{V_{\rm IN}(z)}=\frac{A_{PA}A_{\rm IA}H_{\rm ADC}(z)}{(1+A_{\rm IA}H_{\rm ADC}(z)K_{\rm DAC}(z)H(z))} \quad (1)$$

where A_{PA} is pre-amplification gain outside the feedback loop, $A_{\rm IA}$ is the instrumentation amplifier gain, $K_{\rm DAC}(z)$ is the DAC gain, and $H_{\rm ADC}(z)$ is the transfer function of the ADC. Thus, the transfer function from the electrode to the low-pass filter output is simply

$$G_{\rm LFP}(z)=\frac{V_{\rm LFP}(z)}{V_{\rm IN}(z)}=\frac{A_{PA}A_{\rm IA}H_{\rm ADC}(z)H(z)}{(1+A_{\rm IA}H_{\rm ADC}(z)K_{\rm DAC}(z)H(z))}. \quad (2)$$

$H(z)$ can be designed by starting with a closed-loop prototype $G_{\rm SPK}(z)$. Assuming known $A_{\rm IA}$, $K_{\rm DAC}(z)$, and $H_{\rm ADC}(z)$ (which can be obtained through calibration), one obtains

$$H(z)=\frac{A_{PA}A_{\rm IA}H_{\rm ADC}(z)-G_{\rm SPK}(z)}{A_{\rm IA}H_{\rm ADC}(z)K_{\rm DAC}(z)G_{\rm SPK}(z)}. \quad (3)$$

If we assume for the sake of illustration that $K_{\rm DAC}(z) = H_{\rm ADC}(z) = A_{PA} = A_{\rm IA} = 1$, any invertible prototype $G_{\rm SPK}(z) = N_{\rm SPK}(z)/D_{\rm SPK}(z)$ can be realized by setting $H(z) = (D_{\rm SPK}(z) - N{\rm SPK}(z))/N_{\rm SPK}(z)$. In practice, the ADC and DAC typically introduce additional delays. For the more general case of $H_{\rm ADC}(z) = z^{-N}$, $K_{\rm DAC}(z) = z^{-M}$, we find

$$H(z)=\frac{z^N D_{\rm SPK}(z)-z^{M+N}N_{\rm SPK}(z)}{N_{\rm SPK}(z)}. \quad (4)$$

This $H(z)$ is causal for all open-loop prototypes whose $\deg(D_{\rm SPK}) = \deg(N_{\rm SPK}) + M$, where the $M + N$ leading terms of $N_{\rm SPK}(z)$ and $D_{\rm SPK}(z)$ are equal. Furthermore, the roots of $N_{\rm SPK}(z)$ are still required to lie within the unit circle to ensure stability. If the loop is closed on-chip, $K_{\rm DAC}(z) = K_{\rm ADC}(z) = z^{-1}$ can be achieved, and in this case it is relatively straightforward to find an $H(z)$ that will result in the desired closed-loop transfer function.

For larger values of M and/or N, it becomes increasingly difficult to find an open-loop prototype satisfying the above constraints. In this case, the feedback filter can be designed by guaranteeing that there is sufficient phase margin at the unity-gain frequency of the loop. If there is insufficient phase margin to design a second-order filter, a stable first-order high-pass filter can be built using integrative feedback. The first-order closed-loop transfer function still provides dynamic range reduction in the spike path, and, if additional filtering is needed, it can be provided outside the feedback loop in order to preserve stability.

III. Circuit Design

The neural implant environment is battery-free, and as a result, the supply voltage for the implant becomes a design parameter that is chosen based on tradeoffs in the power-transfer, digital, and analog sections. Given the low clock speed and fine line process adopted, a low supply voltage is preferred for the digital section. For the power transfer section, reducing the required output $V_{\rm DD}$ reduces the number of rectification stages, leading to overall lower area [14]. It is therefore highly desirable for the analog circuits to operate from a low supply as well.

Although designing low-power, high-dynamic-range circuits at low supply voltages is generally very challenging, these difficulties are mitigated in this context by two facts. First, since neural signals have a fixed low-amplitude input swing, amplifier swings can be reduced together with the supply. Because current consumption is determined by an absolute thermal noise

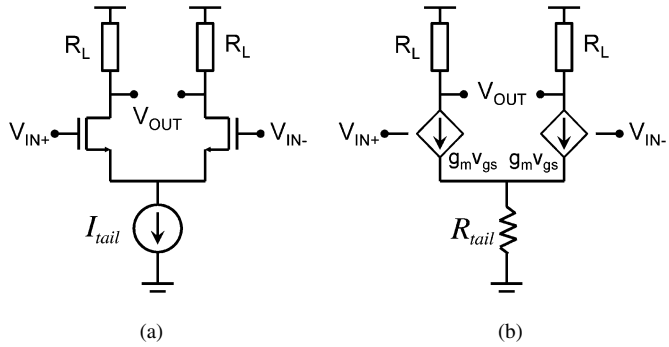

Fig. 8. (a) Resistively loaded differential pair and (b) corresponding small-signal model.

specification, analog power consumption is reduced with decreased $V_{\rm DD}$. Second, the proposed architecture employs global mixed-signal feedback to reduce the dynamic range of each individual gain stage, and enables the use of open-loop circuit techniques that scale more gracefully to a low-supply environment. Based on these considerations, we designed the acquisition chain to operate from a 0.5 V supply. Despite the architectural optimizations, circuit-level techniques are still required to enable state-of-the-art performance and power consumption at low supply voltage. These techniques will be described in the remainder of this section.

A. Low-Noise Offset Cancellation

A key challenge in the design of this dc-coupled acquisition chain is to accommodate the large input offset without degrading common-mode rejection ratio (CMRR) or noise/power efficiency. In order to understand the tradeoffs between offset rejection, common mode rejection, and noise performance, consider the simple differential amplifier of Fig. 8. Input offset voltage $(V_{\rm IO})$ coming from the electrodes changes the relative transconductance (Δg_m) and the relative drain current (ΔI_D) of the left and right halves of the circuit, resulting in $\Delta g_m/g_m = \Delta I_D/I_D = V_{IO}g_m/I_D$. Assuming that all devices are matched and that the product $V_{IO}g_m/I_D$ is small, it can be shown that in the presence of input offset

$$\mathrm{CMRR} = \frac{g_m}{\Delta g_m/(1+2g_mR_{\rm tail})} = \frac{1+2g_mR_{\rm tail}}{V_{\rm IO}g_m/I_D}. \qquad (5)$$

For low supply voltages, the achievable $g_mR_{\rm tail}$ product is limited, and thus the product $V_{\rm IO}g_m/I_D$ must be minimized. This optimization would lead to a design that must use a small amplifier g_m/I_D and would hence degrade the amplifier's noise/power tradeoff. The tight constraints on input-referred noise and leakage current flowing toward the electrode prevents the use of offset cancellation at the input of the instrumentation through a G_m-based servo loop. Canceling the offset at the output of the amplifier as shown in Fig. 9(a) does not solve this problem. Under these conditions, the transconducting stage still processes both signal and offset, and additional noise is introduced by the offset suppression circuitry. It is therefore highly desirable to find an alternative means of offset cancellation.

In order to arrive at such a solution, consider the offset-cancellation scheme originally introduced in [15] and shown in Fig. 9(b). In this design, the offset is cancelled by varying the tail current ratios between two asymmetrically sized differential pairs. In utilizing this topology, we incur a noise penalty associated with offset cancellation from the tail current devices whose noise current travels in asymmetric paths to the output, increasing the total noise.

Fig. 9(c) shows an alternative solution based on a single differential pair with transistors of programmable widths biased in subthreshold. This amplifier has an input-referred offset of

$$V_{\rm off,in} = n\frac{kT}{q}ln\left(\frac{W_{M1}}{W_{M2}}\right) \qquad (6)$$

where kT/q is the thermal voltage, $n = 1+C_{\rm dep}/C_{\rm ox}$ is the subthreshold slope multiplier, and W_{M1} and W_{M2} are the widths of the input devices M_1 and M_2. A feedback loop can then change the relative size of the two transistors comprising the differential pair until the offset introduced by the asymmetry is equal and opposite to the electrode offset. At this point, the tail current and its associated noise current is split equally between transistors M_1 and M_2, $I_{D1} = I_{D2} = I_{\rm tail}/2$, and, because of subthreshold operation, $g_{m1} = g_{m2} = I_{\rm tail}q/(2nkT)$. In order to verify the improved noise performance of the proposed offset cancellation scheme, the input-referred noise density of the three offset cancellation solutions in Fig. 9 are compared in Fig. 9(d). To first order, the solution of Fig. 9(c) cancels the input offset without any penalty in thermal noise or common-mode rejection and was hence adopted in this work. We now proceed to analyze the design in detail for this solution, which we will refer to as a merged amplifier-DAC.

B. Transfer Characteristic Linearization

To cancel $\pm$50 mV of input-referred offset, a W_{M1}/W_{M2} ratio of 4 is required. A linear transfer function of input-referred offset versus DAC code results in a 7-bit DAC requirement to cancel the offset down to sub-1 mV levels. However, if the DAC is thermometer coded, the transfer function is defined by (6) and is thus nonlinear. If W_{M1}/W_{M2} increases linearly, the input-referred offset will change with a steeper slope at the center codes, and then it will towards the edges the transfer curve, requiring higher DAC resolution for a given LSB size. To decrease the resolution requirement, a nonlinear coding scheme is employed. Ideal linearization can be achieved by coding the elements with exponentially increasing size. Since this sizing would result in an impractical layout, the elements were instead coded with increasing unit size in groups. Such an implementation results in a linearized transfer function with built-in DNL, which was designed to be less than 0.25 LSB, corresponding to a maximum input-referred offset of 1 mV and reduced the resulting resolution by 1 b. The transfer characteristic exhibits linear temperature dependence; however, since the power consumption of an implanted IC must be very low and since the human body is a relatively temperature stable environment, even if a 5° change were observed, then $\Delta T/T = 5$ K/310 K, resulting in only a 1.6% change in LSB size of the DAC. The unit-element-sized transfer function and the resulting linearized transfer function

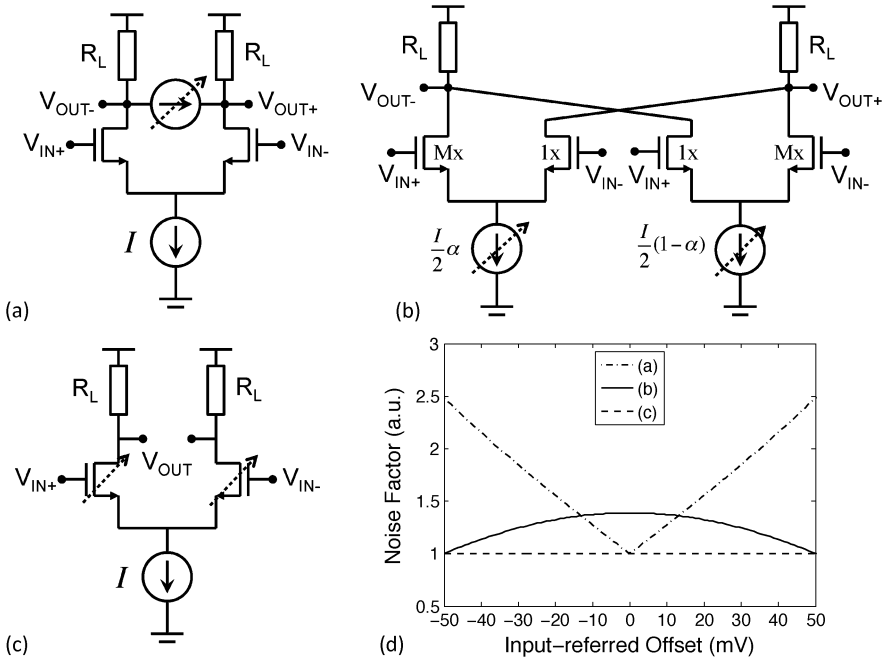

Fig. 9. (a)–(c) DACs used for offset cancellation and (d) a comparison of noise factor versus input-referred offset for DACs (a)–(c) in weak inversion.

are plotted together with the measured results in Fig. 17 as part of Section V. To extend the offset cancellation range beyond ± 50 mV, a larger ratio of W_{M1}/W_{M2} may be employed.

C. Residual CMRR

The first-order analysis presented above assumes that the electrodes contribute the entire input-referred offset of the system. In reality, the devices comprising the amplifier also contribute offset. Threshold voltage mismatch from the differential pair devices, typically much smaller than the electrode offset, appears in series with the electrode offset and is therefore cancelled by the feedback DAC. However, load resistor mismatch cannot be neglected. For a relative load resistor mismatch $\Delta R/R$, nulling the total input-referred offset requires differential pair currents to be imbalanced an amount $\Delta I/I = -\Delta R/R$, leading to an increase in Δg_m. Even in the absence of random mismatch, device subthreshold slope factor n also depends on bias point [16], leading to an additional increase in Δg_m of the input devices after offset cancellation. The variation of n can be decreased by decreasing the inversion coefficient (by increasing W/L) of these devices at the cost of increased area and gate leakage. Finally, since offset cancellation is performed with finite resolution, there is a residual input-referred offset due to the minimum quantization step $V_{\rm LSB}$. The CMRR expression from (5) including all of these effects becomes

$$\mathrm{CMRR} = \frac{1 + 2g_m R_{\rm tail}}{\frac{\Delta R}{R} + \frac{\Delta n}{n} + \frac{V_{\rm LSB} g_m}{I_D}}. \tag{7}$$

While the first and third terms of the denominator are random in nature, the $|\Delta n/n|$ term is deterministic and increases with offset value. CMRR is therefore maximum at $V_{\rm IO} \sim 0$ and progressively degrades as larger values of offset are canceled.

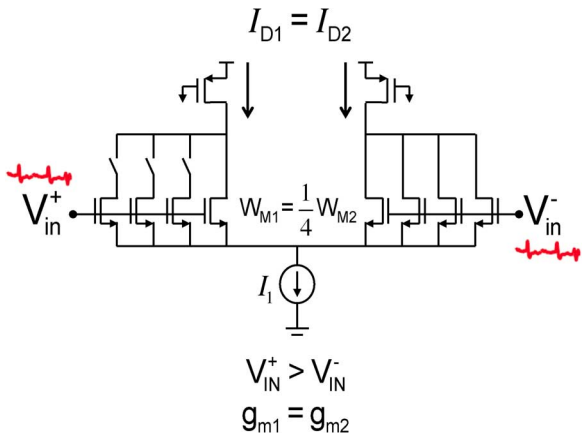

Fig. 10. Operation of the offset cancellation amplifier-DAC in the presence of a large positive input offset.

D. Offset-Dependent $1/f$ Noise

While the chosen amplifier-DAC topology achieves offset-independent thermal noise, the $1/f$ noise corner is modulated as the effective device width and inversion level of the input pair is changed. Consider the merged amplifier-DAC circuit of Fig. 10 in the presence of a positive offset voltage $V_{\rm IO}$ and in the absence of any resistor mismatch. After offset cancellation, we have $NW_{M1} = W_{M2}$ where $N = \exp[|V_{\rm IO}|/(nkT/q)]$. If we call i_{n1}, and i_{n2} the noise generators associated with M_1 and M_2, respectively, then the differential noise current power spectral density can be calculated to be $i_{no} = i_{n1} + i_{n2}$. Since the flicker noise corner of M_1 is N times larger than that of M_2, the flicker noise corner of i_{no} becomes $(N+1)/2$ times larger than that associated with M_1 alone. Expressing the tradeoff in terms of V_{IO}, we find that the $1/f$ noise corner frequency (f_k) becomes

$$f_k = \frac{f_{k0}}{2}\left(1 + \exp\left(\frac{|V_{\rm IO}|}{nkT/q}\right)\right) \tag{8}$$

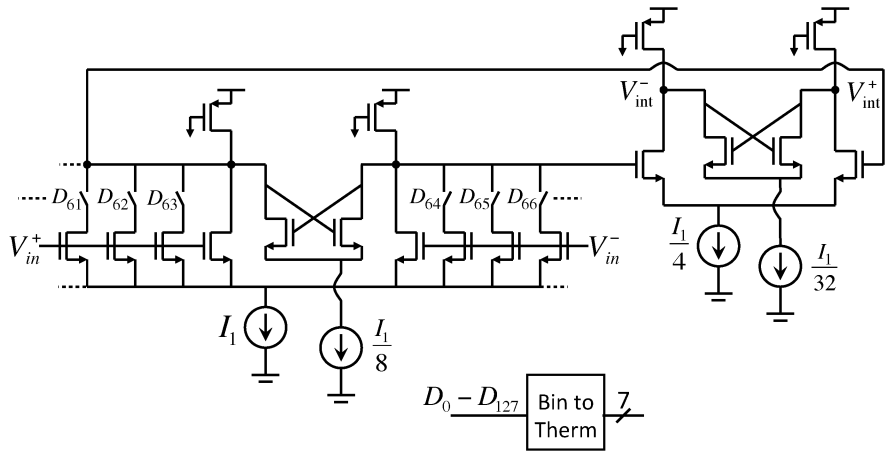

Fig. 11. Complete circuit implementation of merged amplifier-DAC.

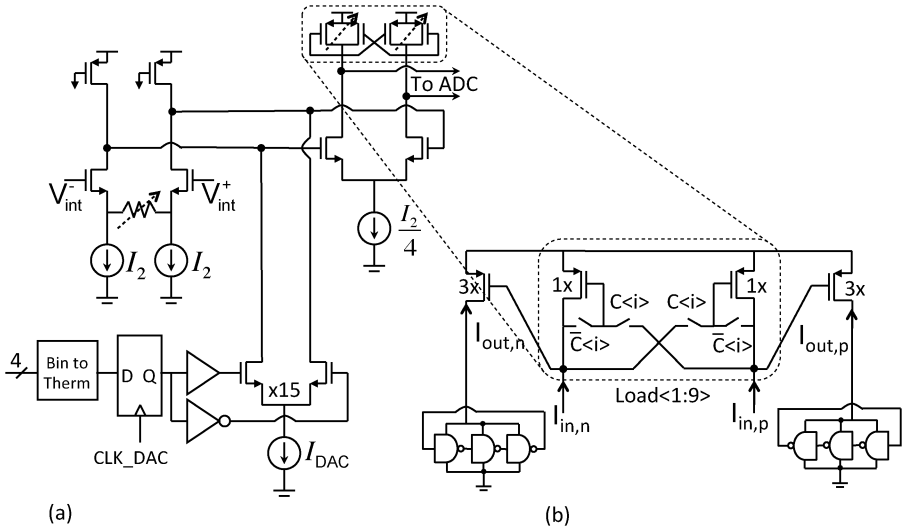

Fig. 12. (a) Circuit diagram of current–feedback DAC and amplfier. (b) ADC driver current mirror with adjustable gain.

where f_{k0} is the flicker noise corner at zero input offset. For a maximum offset of 50 mV, the $1/f$ corner frequency of the input devices is increased by 2.5 times. This increase was accounted for in this design by correspondingly over-designing the device size and the increase in input capacitance was found to have no effect at the frequencies of interest.

The circuit schematic of the designed merged amplifier-DAC is shown in Fig. 11. A two-stage open-loop topology is used to achieve power-efficient gain at low supply voltage. A bias current of 6.4 μA is used in the first stage to meet the thermal noise specification. Input device channel length is set to 0.25 μm for improved output resistance, while the total widths of the input devices are set to 336 μm to keep the $|\Delta n/n|$ factor below 5%. The second stage is scaled to 1/4 the power dissipation of the first stage to save power since noise constraints are relaxed. Both stages employ weak cross-coupled pairs to boost the gain [17] of each stage to 16 dB to give a total LNA gain of 32 dB. The total noise spectral density of the amplifier-DAC referred to the electrodes at $V_{\rm IO} = 0$ is 48 $nVrms/\sqrt{Hz}$, with a 6 kHz $1/f$ corner.

E. Summing Amplifier and DAC

A complete schematic of the second summing amplifier is shown in Fig. 12(a). This stage subtracts the feedback signal from the output of the first stage, which contains an amplified version of the spikes, LFPs, and residual offset. Because of the preceding 30 dB of gain, linearity in this stage is a more pressing concern than noise. A differential amplifier with a differentially connected degeneration resistor and triode transistor loads realizes the amplification stage. Feedback signal subtraction is performed at the output of the amplifier in the current domain by a current-steering DAC. This 9-bit DAC is realized as a 100× oversampled ($f_{ck} = 100$ fs $= 2$ MHz, where f_s is the ADC sample clock frequency), 4-bit structure with first order Delta-Sigma encoding. A thermometer coding scheme and unit element sizing are used to achieve 9-bit linearity. While using four physical bits results in an area penalty compared with a 1-bit implementation, it reduces the input voltage range to the ADC without having to implement an explicit low-pass filter in the analog domain.

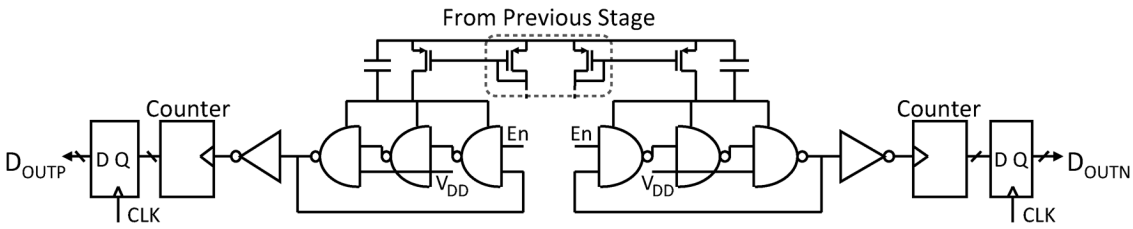

Fig. 13. Circuit diagram of ring-oscillator-based ADC.

The system employs a current-driven, ring-oscillator-based ADC [18], [19] whose linearity requirements are relaxed since it handles only the signal after LFP subtraction. The driver consists of a differential-pair V–I converter cascaded with a current-mode programmable gain block [Fig. 12(b)]. The V–I converter load is comprised of nine pairs of unit pMOS devices that can be individually connected either as cross-coupled pairs or as diode-connected devices. When N devices are cross-coupled, the differential mode load impedance seen by the V–I converter equals $1/(9-N)/g_{mp}$ ($N<5$ to maintain stability). The outputs of this block are connected to the gates of 3 matched unit pMOS devices. Changing N can therefore program the differential-mode current gain without changing the power dissipation, enabling ease of compensation for varying input amplitudes, which are associated with the distance between the neuron and electrode.

The total noise spectral density of the summing amplifier and the ADC driver, referred to the electrodes, is 5 $nVrms/\sqrt{Hz}$, with a 5-kHz $1/f$ corner at a bias current of 1.25 μA (800 nA summing amplifier, 200 nA ADC driver, 250 nA feedback DAC).

F. Analog-to-Digital Converter

In order to keep the quantization noise well below the thermal noise floor an ADC resolution of at least 8 bits is required. The ADC employs a pseudo-differential, VCO-based architecture shown in Fig. 13. The positive and negative driver output currents are used as the bias for two single-ended, three-stage CMOS ring oscillators realized with NAND gates, which feed the clock inputs of 9-bit digital counters. Simple CMOS rings are used to minimize power and area, so that differential operation is required in order to provide suppression of supply and common-mode disturbances. Driving the ADC in the current domain through a pMOS current mirror further improves PSRR and soft-rail operation maintains good linearity through the full dynamic range [20]. While extra resolution can be obtained by sampling all of the oscillator phases [21], the intrinsic speed of the 65 nm CMOS technology used is such that the desired 8 bits, 20 kS/s is easily achieved with a single-phase measurement. Each oscillator is designed such that the minimum and maximum oscillation frequencies $f_{\min}$ and $f_{\max}$ satisfy $|f_{\max}-f_{\min}|>2^8\cdot f_s$ with $f_s=$ 20 kHz, therefore each differential output results in an 8-bit dynamic range for a total of 9 bits of quantization.

The counter output represents the average oscillator frequency over a period, corresponding to integration in the time domain and a sinc transfer function in the frequency domain. Thus, the converter provides the desired boxcar sampling response, preventing aliasing of the wideband noise from the instrumentation amplifier. Sinc filters have been used as anti-aliasing filters in this context [22] but with large-area analog implementation; this work merges this anti-aliasing filter into the ADC in a compact form factor. The box-car sampling characteristic introduces a second key benefit in this system, as it suppresses the shaped quantization noise from the Delta-Sigma ($\Delta\Sigma$) DAC employed for LFP cancellation. Because of the harmonic relation between the $\Delta\Sigma$ clock and the ADC clock, and the integrating nature of the ADC, the transfer between quantization noise and ADC output $\mathrm{NTF}_Q(z)$ expressed in the 2 MHz clock domain is given by the modulator NTF cascaded with that of a 100 tap moving average (MA) filter. For a $\Delta\Sigma$ noise transfer function of $\mathrm{NTF}(z)=1-z^{-1}$, and

$$\mathrm{NTF}_Q(z)=\mathrm{NTF}(z)MA(z)=\frac{1-z^{-100}}{100}. \tag{9}$$

Essentially, the integrating characteristic of the ADC averages the DAC output bit-stream while performing the conversion, acting as first stage of decimation. As a result, the high-frequency quantization noise from the $\Delta\Sigma$ modulator is greatly attenuated at the output port and does not degrade the overall system SNR.

IV. Measurement Results

The chip was fabricated in a 65 nm 1P7M LP CMOS process from ST Microelectronics. A chip microphotograph is shown in Fig. 14. The chip contained two channels and one stand-alone ADC test block. The inset shows the detailed layout of a single channel. The total chip area is pad-limited to 1.2 mm $\times$ 1.2 mm, while the core channel area is 80 μm $\times$ 170 μm. The chip power consumption was measured to be 5.04 μW. Electrical characterization of the chip was performed by housing the die in a 48-pin 7 mm $\times$ 7 mm metal lead frame package connected a PCB through a test socket. The digital filters, which form the feedback path for LFP separation, were implemented off-chip on an FPGA. Fig. 15 shows a complete diagram of the implementation, and Table I shows the area and power breakdown by block. The total area of the channel includes the 0.0017 mm^2 required to synthesize the off-chip digital filters. All measurements were performed through the full acquisition channel including the on-chip ADC. Post-processing of the digital outputs was performed using MATLAB. Differential sine wave inputs were produced using a Stanford Research Systems DS360 low-distortion signal generator and attenuated to proper input levels at the acquisition channel input.

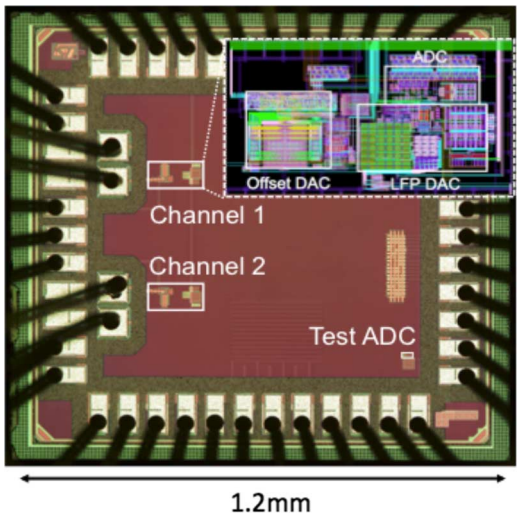

Fig. 14. Chip microphotograph.

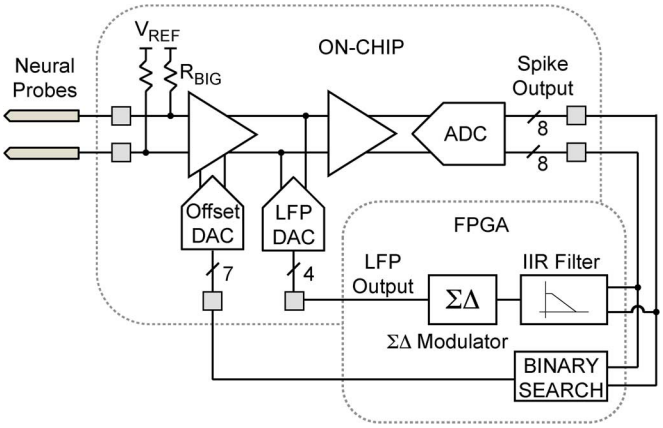

Fig. 15. System diagram.

TABLE I
POWER AND AREA BREAKDOWN BY BLOCK

	Power	Area
Merged Amplifier-DAC	4.13μW	0.0037mm^2
Summing Amplifier & DAC	0.66μW	0.0045mm^2
ADC	0.24μW	0.0018mm^2
Digital Filters	0.1μW*	0.0017mm^2

* Estimated.

The measured closed-loop transfer functions of the IC from the input to the spike and LFP outputs are shown in Fig. 16. The transfer function of the spike band shows a 300 Hz high-pass cutoff, set by the digitally programmable feedback loop. The full-scale voltage of the spike transfer function is programmable between 870 μV and 3.5 mV. The high-frequency rolloff is due to the sinc transfer function of the A/D converter. This droop is deterministic and can be compensated for in DSP if needed. The loop filter order was limited to be first-order by the latency introduced by implementing the filters off-chip. Further filtering the two signals outside the feedback loop will enhance signal band isolation. If the digital signal processing were integrated

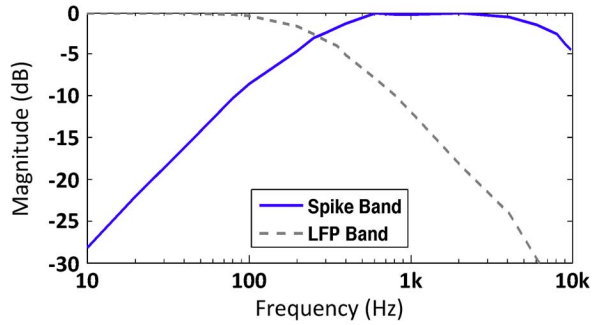

Fig. 16. Normalized magnitude plot of closed-loop system.

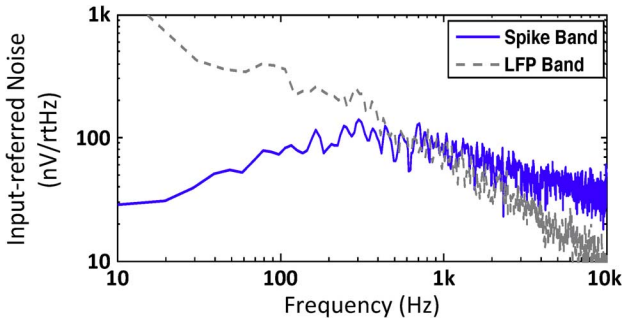

Fig. 17. Input-referred noise spectral density in Spike and LFP bands.

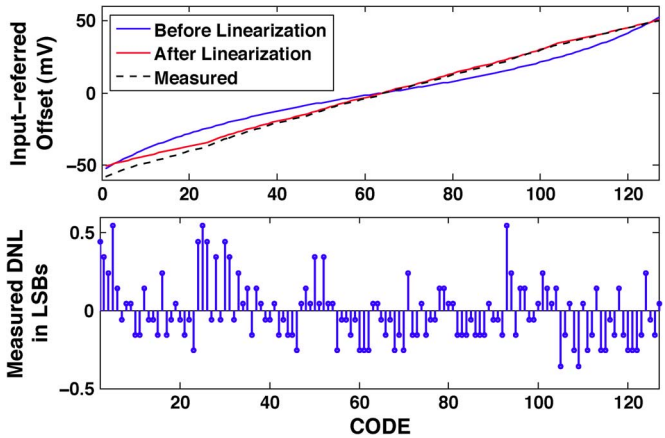

Fig. 18. Merged amplifier-DAC transfer curve (top) and DNL (bottom).

on-chip, higher filter order could also be implemented inside the feedback loop.

The measured input-referred noise is shown in Fig. 17 over the same bandwidth. The measured integrated noise in the spike band is 4.9 μVrms in a 10 kHz bandwidth, while the LFP band has a noise floor of 4.3 μVrms in a 300 Hz bandwidth. At low frequency, both neural signals and transistors exhibit a $1/f$ power spectrum; therefore the low-frequency LFP band can absorb larger noise spectral density while maintaining SNR [23]. $\Delta\Sigma$ quantization noise was not observed and is therefore suppressed below thermal noise levels.

Fig. 18 shows the measured performance of the offset-cancellation amplifier-DAC. The top shows the measured transfer curve between digital code and input-referred offset. This curve closely matches that predicted by (6). DNL is plotted at the bottom of Fig. 18. Since the maximum measured DNL and

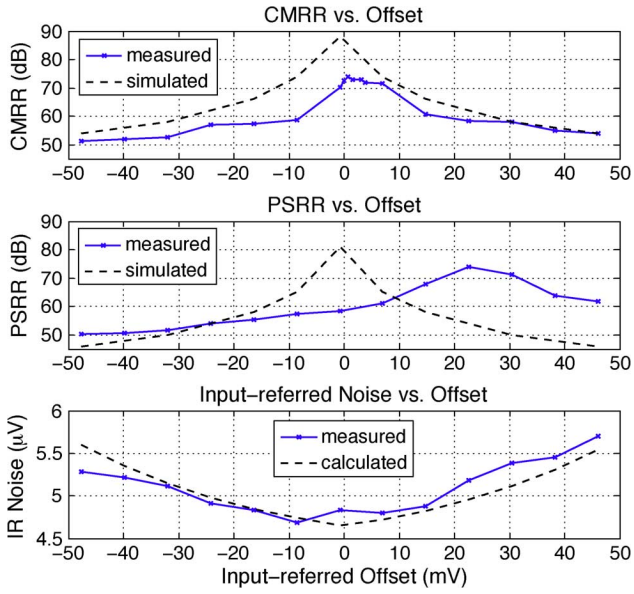

Fig. 19. CMRR (top), PSRR (center), and input-referred integrated noise (bottom) versus input-referred offset.

LSB sizes are 0.55 LSB and 0.8 mV, respectively, the maximum input-referred offset after the first stage of cancellation is 1.2 mV. Excess DNL was observed at the lower extreme of offset cancellation and was found to be systematic across multiple chips due to asymmetry in the layout.

Fig. 19 shows the measured and simulated CMRR (top) and PSRR (center). Input-referred noise (bottom) is plotted together with calculated values. Each is plotted as a function of the initial input offset after rebalancing the amplifier. Values remain above 50 dB for both CMRR and PSRR for all values of offset. Peak PSRR is shifted from the center due to sensitivity to mismatch in the second stage of amplification, while the input differential pair dominates CMRR. The noise is measured through the on-chip ADC and therefore includes quantization noise. Input-referred noise stays below 6 μVrms for all conditions and below 5 μVrms for $\pm$20 mV of offset. Acute *in vivo* measurements showed that offsets were rarely above 20 mV, although long-term studies have yet to be done. Note that, since the simulated $g_m R_{\text{tail}}$ product for this amplifier is only 26 dB, a solution employing output offset cancellation would require an impractical $g_m/I_D = 1.6$ to achieve the same worst-case CMRR.

Fig. 20 shows the measured output spectrum of the acquisition system for a 200 μVrms input sine wave. Two percent total harmonic distortion (THD) is observed for the entire channel at the maximum system gain. Fig. 21 shows the measured output spectrum of the stand-alone ADC test structure. The spectrum shows an SNDR of 45 dB and an SFDR of 58 dB, a linearity that is sufficient for 9-bit operation. The converter consumes 240 nW, which corresponds to a figure of merit of 84 fJ per conversion step. First-order quantization noise shaping is observed.

The system was further verified through *in vivo* measurement. The inputs of the chip were connected to a microelectrode array implanted near the motor cortex of a live, awake, free-moving rodent two months prior to recording. Fig. 22 shows the

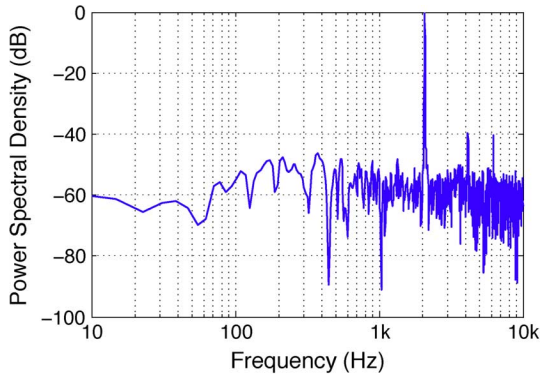

Fig. 20. Power spectral density of system with a 200 μVrms, 2 kHz sine wave input.

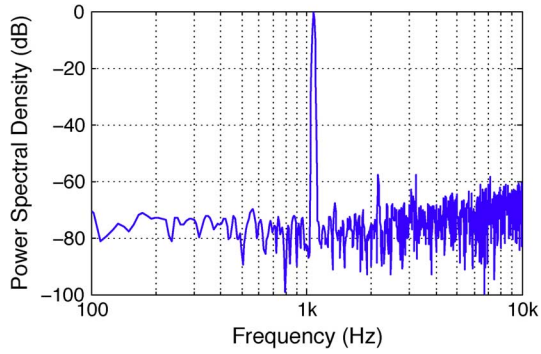

Fig. 21. Power spectral density of ADC with 1 kHz sine wave input at full scale.

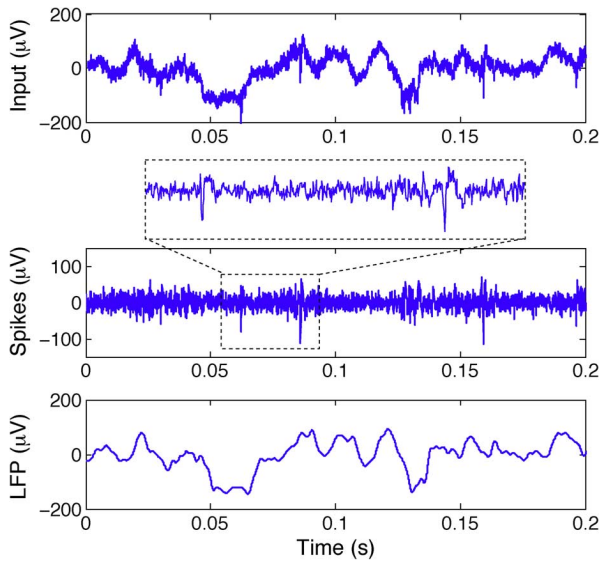

Fig. 22. *In vivo* recordings from live rodent: input waveform (top), Spike output (middle), and LFP output (bottom).

recorded waveform from one of the trials. The measurements show good quality recordings and indicate that dc coupling the chip to the electrode array does not have significant impact on signal integrity. The finite leakage between LFP and spike band is due to the first-order rolloff of the loop filter.

Table II summarizes the performance of this work as compared to state of the art designs from industrial and academic

TABLE II
SUMMARY OF PERFORMANCE METRICS FOR THIS WORK AND COMPARISON WITH THE STATE OF THE ART. ALL METRICS FOR THIS WORK ARE GIVEN FOR A COMPLETE SYSTEM INCLUDING ADC

	[3] JSSC '09	[4] JSSC '07	[6] BioCAS '07	[7] ISSCC '10	[24] VLSI '11	This Work
Power (μW)	15	42.2	7.56	0.64	43	**5.04**
IRNoise (μV), Spike	7.0	5.1	3.06	14	2.2	**4.9**
Spike Bandwidth	5kHz	5kHz	5.3kHz	6.2kHz	10kHz	**10kHz**
NEF	4.6	9.8	2.67	6.5	5	**5.99**
$NEF^2 \cdot V_{DD}$	63.48	316.9	20	33.8	30	**17.96**
IRNoise (μV), LFP	-	-	1.66*	-	14	**4.3**
LFP Bandwidth	-	-	300Hz*	-	100Hz	**300Hz**
CMRR (dB)	-	-	66	59	-	**75**
PSRR (dB)	-	-	75	71	-	**64**
V_{DD} (V)	3	3.3	2.8	0.8	1.2	**0.5**
Area (mm^2)	0.04	0.16	0.16	0.4**	0.2**	**0.013**
Technology	0.35μm	0.5μm	0.5μm	0.13μm	0.13μm	**65nm**
Blocks included in comparison	LNA, BPF	LNA, BPF	LNA, BPF	LNA, BPF	LNA, BPF, ADC	**LNA, BPF, ADC**

*LFP not recorded simultaneously, requires reconfiguration
**estimated

* LFP cannot be recorded simultaneously with Spikes.
** Estimated.

researchers [3], [4], [6], [7], [24]. By carefully engineering the system architecture to exploit the strength of deep-submicron processes, and employing low-noise circuit techniques, the area of the entire acquisition chain is reduced to 0.013 mm^2, over a factor of 3 smaller than the smallest front-end amplifier reported to date [3]. State-of-the art noise, CMRR and PSRR are maintained despite the reduction of the supply to 0.5 V.

A. Comparison Metric

The fourth and fifth rows of the table compare the measured power-consumption and noise tradeoff achieved by this work to state of the art. This comparison is made using the well-established noise efficiency factor (NEF) [25] metric, as well as a power efficiency factor metric $\mathrm{PEF} = \mathrm{NEF}^2 V_{\mathrm{DD}}$. NEF normalizes the input-referred noise of the amplifier to the input-referred noise of a single BJT which dissipates the same total current. For two circuits with the same supply voltage, NEF is a good metric to describe the power/noise tradeoff. However, two amplifiers with the same total current and noise but different V_{DD}s will have equal NEF but different power dissipation, therefore NEF is insufficient to describe which is more power efficient. To mitigate this issue a more direct comparison of the total power consumption can be made by the PEF metric, which normalizes the noise power times the total power

$$\mathrm{PEF} = \frac{V_{n,\mathrm{rms}}^2 \cdot V_{\mathrm{DD}} I_{\mathrm{tot}}(myckt)}{V_{n,rms}^2 \cdot V_{\mathrm{DD}} I_{\mathrm{tot}}(\mathrm{bjt})} = \frac{V_{n,\mathrm{rms}}^2 \cdot 2P_{\mathrm{tot}}}{\pi \cdot kT/q \cdot 4kT \cdot \mathrm{BW}} \tag{10}$$

The resulting metric is dependent on the bandwidth, input-referred noise, and power of the circuit rather than the current. NEF and PEF numbers for this work were computed using the total input-referred noise and power of the entire signal acquisition chain including the ADC. Typically, NEF is computed only for the amplifier and therefore does not describe the efficiency of the entire system, however, the NEF of the merged amplifier-DAC is 5.3 and the PEF is 14. When compared using the NEF metric, the proposed system is comparable to recent state of the art. When comparing systems using the PEF metric, this work is the most power-efficient reported.

V. CONCLUSION

Compact neural acquisition systems are an integral part of future wireless brain-machine interfaces. This work combines dc-coupled inputs with an architecture that uses mixed-signal feedback for filtering and offset suppression to achieve a compact area, while providing per-pixel digitization and simultaneous LFP and spike recording. The optimized architecture is combined with a merged instrumentation amplifier-DAC that enables noise-efficient offset cancellation and with a boxcar sampling ADC to obtain state of the art performance in an energy efficient manner while requiring only a 0.5 V supply.

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