24.1 A Miniaturized 64-Channel 225μW Wireless Electrocorticographic Neural Sensor

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Substantial improvements in neural-implant longevity are needed to transition brain-machine interface (BMI) systems from research labs to clinical practice. While action potential (AP) recording through penetrating electrode arrays offers the highest spatial resolution, it comes at the price of tissue scarring, resulting in signal degradation over the course of several months [1]. Electrocorticography (ECoG) is an electrophysiological technique where electrical potentials are recorded from the surface of the cerebral cortex, reducing cortical scarring. However, today's clinical ECoG implants are large, have low spatial resolution (0.4 to 1cm) and offer only wired operation.

To enable chronic and stable neural recording, we introduce a minimally invasive, wireless ECoG microsystem. Wireless powering and readout are combined with a microfabricated antenna and electrode grid that has >10× higher electrode density than clinical ECoG arrays, providing spatial resolution approaching today's penetrating electrodes. Area- and power-reduction techniques in the baseband and wireless subsystem result in over 10× IC area reduction with a simultaneous 3× improvement in power efficiency over the state of the art (see Fig. 24.1.4), enabling a minimally invasive platform for 64-channel recording. The low power consumption of the IC, together with the antenna integration strategy enables remote powering at 3× below established safety limits [2], while the small size and flexibility of the implant minimizes the foreign body response. The improved implant safety and longevity gives wireless ECoG excellent prospects to become the technology of choice for clinically relevant BMIs in the foreseeable future [1].

Figure 24.1.1 illustrates the concept of the implantable ECoG microsystem and a block diagram of the IC, which includes circuitry for signal acquisition, a matching network, clock recovery, communication and power management. To mitigate the implantation of a large rigid structure, the IC is bonded directly to thin-film platinum and gold electrodes that are patterned over Parylene C, a biocompatible polymer [3]. The highly flexible grid is 10μm thick and conforms to the cortical folds, further reducing neural damage. Platinum black is electroplated onto the electrode surface reducing the impedance to 10kΩ at 100Hz. A 6.5mm-diameter, single-loop antenna is monolithically integrated together with the electrodes and is used for both power and data telemetry. The antenna achieves -17.3dB link gain at 300MHz while transmitting across a human skull model [2]. A 1.5cm-diameter external antenna completes the link and powers the device, radiating 12mW of power, 3× lower than the IEEE and FCC recommendation.

The 64-channel front-end array (with an ADC per channel) dominates the IC power consumption, making a power-efficient design critical. The acquisition of useful ECoG signals necessitates an input-referred noise of ~1μV over 1 to 500Hz, which must be achieved in the presence of a large DC offset (up to ±50mV) at the electrode-chip interface. The key to power-efficient design lies in canceling the DC offset early in the signal chain while minimizing flicker noise. The architecture of Fig. 24.1.2 achieves this by using a chopper-stabilized amplifier to minimize 1/f noise, and an oversampled ΔΣ DAC with 15b resolution to cancel the upmodulated DC offset. To prevent instantaneously large amplifier inputs, 5 physical DAC bits are implemented as a 31-element, thermometer-coded capacitor array with unit capacitor C_{LSB}. $31C_{LSB}=0.1C_{in}$ is chosen to cancel the offset while keeping signal attenuation below 1dB. The large time constants necessary for filtering the offset are implemented digitally [4], enabling an area of 0.025mm² for each front-end. Using an open-loop amplifier improves input impedance, resulting in Z_{in}=28MΩ at 100Hz with f_{chop}=8kHz. After chopper demodulation and RC filtering (to suppress ΔΣ noise), the signal is digitized by a pseudo-differential, VCO-based ADC [4] operating at 1kS/s. The ADC has a raw resolution of 15b to suppress quantization noise while processing the ECoG signal, the chopper ripple, and the ΔΣ noise the DAC. By designing $f_{chop}=Nf_{ADC}$ (N is an integer) the chopper ripple falls in a notch of the ADC sinc transfer function [4] eliminating the need for a ripple-reduction loop.

The 1kS/s, 15b digital outputs are serialized into a 1Mb/s Miller-encoded data stream and back-scattered through a shunt-load modulation switch. We trade off modulation depth in order to support simultaneous data and power transfer and employ a dual-mode RF-to-DC rectifier to handle the input voltage variation. As shown in Fig. 24.1.3, a high-impedance passive rectifier (low-impedance active rectifier) is activated when the data modulated impedance is switched to high (low) impedance. The passive rectifier is implemented using diode-connected transistors, and the active rectifier utilizes a mixed-signal feedback loop to control the timing of the synchronous switches and prevent reverse conduction. This feedback loop replaces the asynchronous gate-driving comparators of conventional active rectifiers and uses clocked comparators operating at 8× lower frequency than the power carrier, reducing power. The dual-mode rectifier efficiency is modulated inversely to the data modulation, and therefore available input power, in order to maintain a constant output power. This technique reduces ripple by 10× at the rectifier output when compared to a single active rectifier and is exploited to reduce the supply decoupling capacitance to 4nF, eliminating the need for external capacitors.

The IC is fabricated in a 65nm 1P7M low-power CMOS process. A chip microphotograph is shown in Fig. 24.1.7. The total chip area is pad-limited to 2.4×2.4mm² and the active circuit area totals 1.72mm², with 1.6mm² occupied by the front-end array. The total power dissipation of the chip is 225μW, including the 60% power conversion efficiency (Fig. 24.1.5).

Figure 24.1.4 shows the measured closed-loop transfer functions of the ECoG front-end from the electrode input to the ADC output. The first-order high-pass pole frequencies are digitally configurable with four such configurations shown. The high-frequency roll-off is due to the sinc transfer function of the ADC. Input-referred noise spectral density is also shown in Fig. 24.1.4 with chopping disabled and for a range of digitally configurable chopper frequencies (and therefore also input impedance). Integrated over 500Hz, chopper stabilization decreases the noise floor by 400×. Comparing this design against state-of-the-art noise- and power-efficient ECoG and EEG front-ends [5-7], the reported techniques enabled a 16× area reduction and a 3× improvement in power efficiency factor (PEF) [4] while integrating an ADC per channel.

In Fig. 24.1.5, the performance of the wireless link is verified by wirelessly transmitting a PRBS-7 data pattern generated on-die. Zero errors were found in 5.9Mb of data resulting in a BER $<1.7\times10^{-7}$ with 1cm antenna separation in air and *in-vivo*. Figure 24.1.5 also shows the 10× reduction in rectifier output voltage (V_{RECT}) fluctuation when switched from single to dual mode operation.

The IC was assembled together with the microfabricated ECoG electrodes and antenna on a PCB and implanted in an anesthetized Long-Evans rat over the left cortical hemisphere. All experiments were performed in compliance with the regulations of the Animal Care and Use Committee at UC Berkeley. Electrical recordings were made on all channels prior to and 15 minutes after the administration of Pentobarbital, a sedative. It is known that anesthesia causes increased δ band (1 to 4Hz) oscillations and depressed high-γ (65 to 125Hz) activity [8]. A representative channel is plotted in Fig. 24.1.6 showing that results are consistent with deepened anesthetic state.

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References:
[1] G. Schalk, "Can Electrocorticography (ECoG) Support Robust and Powerful Brain-Computer Interfaces?" *Frontiers in Neuroeng.*, vol. 3, Jan. 2010.
[2] T. Bjorninen, *et al.*, "Antenna Design for Wireless Electrocorticography." *IEEE AP-S/URSI*, July 2012.
[3] P. Ledochowitsch, *et al.*, "Fabrication and Testing of a Large Area, High Density, Parylene MEMS μECoG Array," *IEEE MEMS Conf.*, 2011.
[4] R. Muller, *et al.*, "A 0.013mm², 5μW, DC-Coupled Neural Signal Acquisition IC with 0.5V Supply." *J. Solid-State Circuits*, vol. 47, no. 1, Jan. 2012.
[5] T. Denison, *et al.*, "A 2μW 100nV/rtHz Chopper-Stabilized Instrumentation Amplifier for Chronic Measurement of Neural Field Potentials." *J. Solid-State Circuits*, vol. 42, no. 12, Dec. 2007.
[6] R.F. Yazicioglu, *et al.*, "A 200μW Eight-Channel EEG Acquisition ASIC for Ambulatory EEG Systems," *J. Solid-State Circuits*, vol. 43, no. 12, Dec. 2008.
[7] F. Zhang, *et al.*, "A Low-Power ECoG/EEG Processing IC With Integrated Multiband Energy Extractor," *IEEE Trans. CAS I*, vol. 58, no. 9, Sept. 2011.
[8] J. Borjigin, *et al.*, "Surge of Neurophysiological Coherence and Connectivity in the Dying Brain," *Proc. Nat. Acad. Sci.*, Aug 2013.

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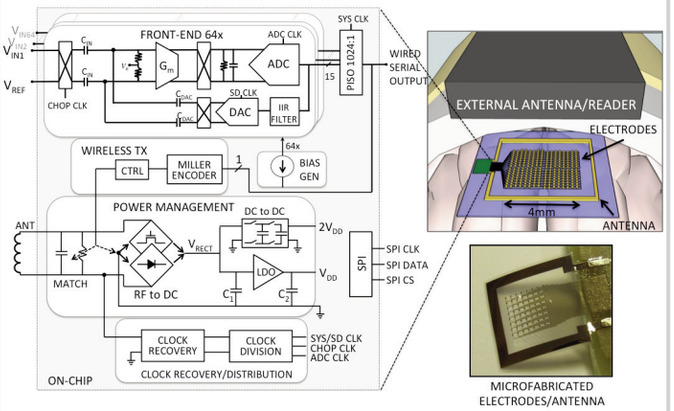


Figure 24.1.1: Device concept for Electrocorticographic (ECoG) neural sensor, IC block diagram, and photograph of the high-density microfabricated electrodes and antenna.

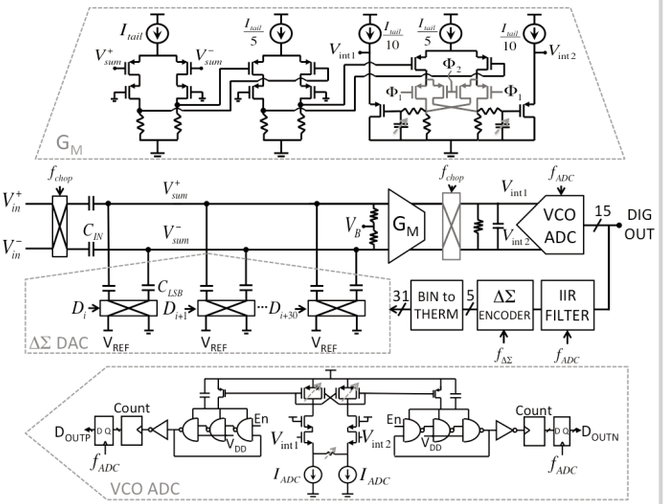


Figure 24.1.2: Detailed front-end circuit diagrams.

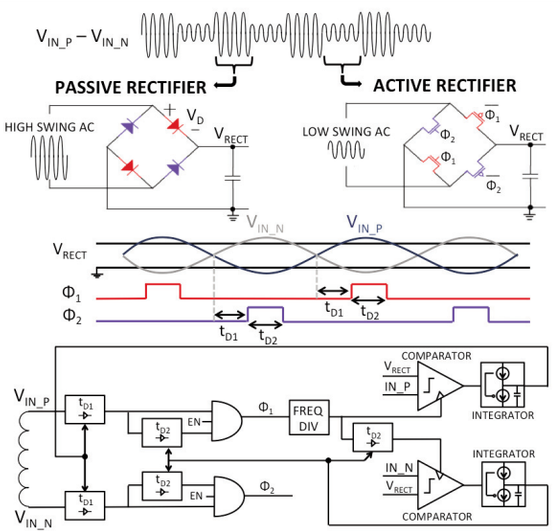
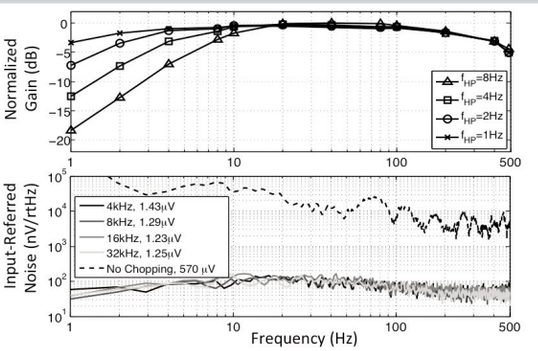
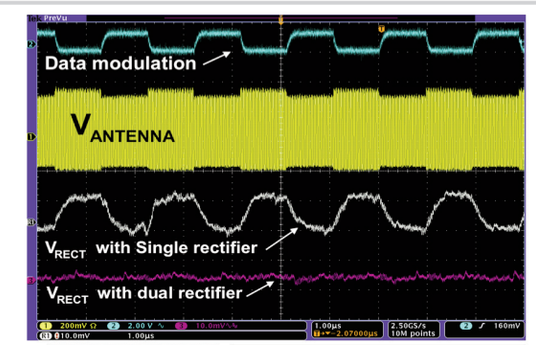


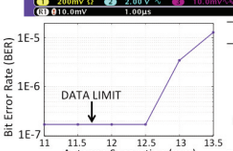
Figure 24.1.3: RF-to-DC rectifier circuit and timing diagrams.



*includes ADC **requires off-chip filter	[5] JSSC '07	[6] JSSC '08	[7] TCAS, '11	THIS WORK
Power (μW/ch)	2	33.3	3.24	**2.3**
IRNoise (nV/rtHz)	100	60	85	**58**
NEF/PEF	4.6/38.1	4.3/55.5	5.38/34.7	**4.76/11.3***
Area (mm²/ch)	0.8	0.5	0.4**	**0.025**
ADC Resolution	none	11-bit	none	**15-bit**
# of Channels	1	8	2	**64**
Technology	0.8μm	0.5μm	0.13μm	**65nm**

Figure 24.1.4: Front-end measurement results of full channel including ADC. State-of-the-art comparison is charted for f_{chop}=8kHz.





	Area (mm²)	Power (μW)
64 FE ARRAY	1.6	147.2
TX & ENCODER	0.015	2.4
CLOCK RECOVERY	0.012	10.6
POWER MANAGMENT	0.09	64.1
TOTAL	1.72	224.3

Figure 24.1.5: Wireless subsystem measurement results: RF-to-DC rectifier output ripple for single and dual-mode rectification during data modulation, BER vs. antenna separation, and power/area breakdowns.

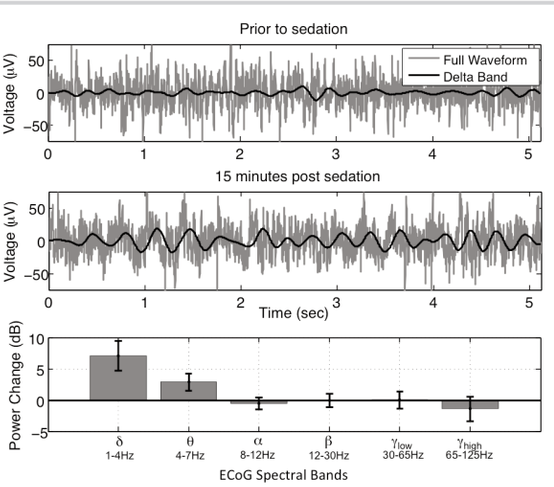


Figure 24.1.6: In-vivo system measurements: recordings from a single channel before and 15 min. after sedative administration. Spectral band power changes are plotted for all channels.

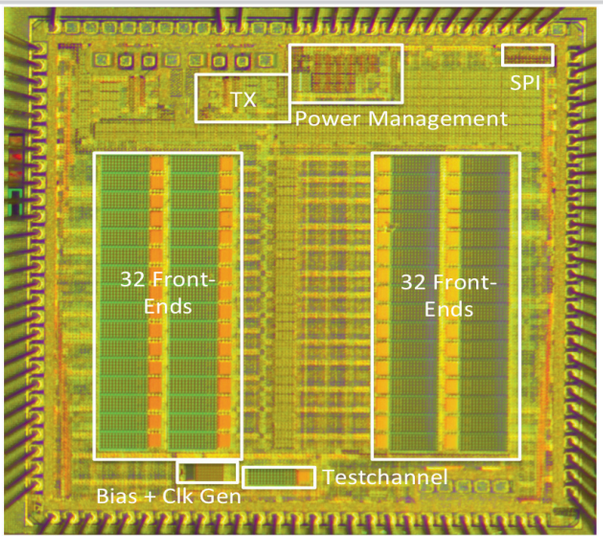


Figure 24.1.7: Chip microphotograph.

