17.2 A 0.013mm² 5μW DC-Coupled Neural Signal Acquisition IC with 0.5V Supply

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Recent success in brain-machine interfaces has provided hope for patients with spinal-cord injuries, Parkinson's disease, and other debilitating neurological conditions [1], and has boosted interest in electronic recording of cortical signals. State-of-the-art recording solutions [2-5] rely heavily on analog techniques at relatively high supply voltages to perform signal conditioning and filtering, leading to large silicon area and limited programmability. We present a neural interface in 65nm CMOS and operating at a 0.5V supply that obtains performance comparable or superior to state-of-the-art systems in a silicon area over 3× smaller. These results are achieved by using a scalable architecture that avoids on-chip passives and takes advantage of high-density logic. The use of 65nm CMOS eases integration with low-power digital systems, while the low supply voltage makes the design more compatible with wireless powering schemes [6].

The chip architecture is shown in Fig. 17.2.1. The input is DC-coupled, and the common mode is stabilized through a large (>1GΩ) on-chip resistor. This saves the area of large (often 10s of pF) AC-coupling capacitors. Since the resistor is not used to form a filter time constant, the system is agnostic to its variations. Mixed-signal feedback is used to cancel the electrode offset and separate the 1-to-300Hz Local Field Potential (LFP) band from the 300Hz-to-10kHz Action Potential (Spike) band. Two separate feedback loops are used: an outer low-noise DAC provides coarse offset suppression at 1Hz or less, while the inner loop performs LFP filtering and fine residual offset correction. The Spikes are available at the output of the ADC while the LFP signal becomes available at the input of the inner DAC. The mixed-signal feedback replaces traditionally analog filters and enables the system to operate with an 8b ADC while digitizing both the Spikes and LFPs. To minimize area and power consumption the feedback is split into a dual-loop architecture which reduces the very large (16b) DAC resolution requirement of filtering the offset and LFP together into two moderate resolution DACs. A low-pass digital IIR filter in the feedback path creates a high-pass filter response to separate the Spike and LFP bands. The closed-loop transfer function can be digitally configured, greatly increasing system flexibility.

Figure 17.2.2 shows the circuit schematics of the individual blocks. The first amplifier (LNA) of the signal chain needs to achieve a low input-referred noise and to provide high enough gain to suppress noise from the subsequent blocks, while rejecting the large electrode offset. At low frequency, both neural signals and transistors exhibit a 1/f power spectrum, therefore the low-frequency LFP band can absorb larger noise spectral density while maintaining SNR [7]. The key challenge is therefore to keep the Spike band noise low. Due to the low supply voltage, cascode topologies are impractical, and hence two differential pairs with PMOS triode loads are cascaded. Weak cross-coupled pairs are used to boost the LNA gain to 32dB. The offset is cancelled by changing the relative widths of the input differential pair transistors. For sub-threshold devices, the input-referred offset is given by Eq. 1:

$$\Delta V_{GS} = n\frac{kT}{q}\ln(k_w) \quad (1)$$

where k_w is the ratio of the widths of the input devices and n is the subthreshold slope factor. For sub-threshold devices g_m is independent of device width, thus the offset is canceled without compromising CMRR while maintaining a gain and input-referred noise voltage independent of DAC code. The measured characteristic of the offset DAC is shown in Fig. 17.2.3. The 7b, thermometer-coded offset DAC uses a nonlinear unit element coding to cancel ±50mV of electrode offset with an LSB of 0.8mV and a maximum DNL of 0.55LSB for a worst-case residual offset of 1.2mV.

Since thermal noise constraints of the second summing stage are relaxed by the gain of the LNA, a straightforward current summing DAC architecture is chosen (Fig. 17.2.2). To keep quantization noise from degrading the system SNR, a dynamic range of 9b is necessary to handle the LFP and residual offset. Oversampling and Sigma-Delta encoding are used to achieve this dynamic range in a small footprint by using a 4b thermometer-coded DAC with first-order noise shaping running at 2MHz.

To achieve minimal area, an 8b counter-based ADC is used (Fig. 17.2.2). The integrating transfer function of this ADC provides anti-aliasing and filters out-of-band noise from the sigma-delta DAC. A pseudo-differential, current driven architecture mitigates supply noise coupling and minimizes distortion [9]. A differential pair is used for V-I conversion, paired with an active load that provides a programmable, linear current-mode gain that tunes the full-scale range of the ADC from 870μV to 3.5mV when referred to the channel input. Measurements of a standalone ADC structure show 7.15 ENOB at 20kS/s with 240nW power consumption, leading to a FOM of 84fJ/step in 0.0018mm².

The prototype was fabricated in a 65nm 1P7M LP-CMOS technology. A microphotograph is shown in Fig. 17.2.7. The overall die area is pad-limited to 1.4mm², while the core channel area is 70×180μm². The entire channel consumes 5.04μW from a 0.5V supply. All signal processing is performed on chip, with the exception of the digital filter, which was implemented on an FPGA. Synthesized, the filter occupies 0.0017mm².

Figure 17.2.4 shows measurements of the closed-loop transfer function of both the LFP and Spike band outputs. The high-pass filter pole location is generated by integrator-based feedback and is digitally tunable. Measurements of the Spike and LFP band noise floors are also shown in Fig. 17.2.4. 4.9μV of input-referred noise is achieved in a 300Hz-to-10kHz bandwidth.

The system was further verified with the sensor in a realistic, 60Hz environment by performing live recordings from the motor cortex of an awake rat. The rat was implanted with two 2×8 Plexon Platinum-Iridium microwire arrays 2 months prior to recording. Figure 17.2.5 shows system outputs with separated Spike band (middle) and LFP band (below.) A high-pass filter pole frequency of 300Hz was chosen.

Figure 17.2.6 shows the performance summary and comparison with state-of-the-art neural signal acquisition systems. For this work, the specifications given in Fig. 17.2.6 are for the entire acquisition chain including the ADC, while the specifications for [2-5] are given for the LNA/Bandpass filter only. The total silicon area of this work is 3× smaller than that of the smallest amplifier previously reported [2]. High CMRR is also maintained despite the low V_{DD}. The power efficiency of this amplifier is compared through both the popular NEF metric [8] and the modified metric,

$$NEF^2 \cdot V_{DD} = V_{rms,in}^2\left(\frac{2P_{tot}}{\pi \cdot kT/q \cdot 4kT \cdot BW}\right) \quad (2)$$

which is dependent on power rather than current. Given that power dissipation in neural amplifiers is typically limited by input-referred noise, and that this design achieves the lowest $NEF^2 \cdot V_{DD}$, utilizing the proposed techniques to reduce area and operating voltage does not come at the cost of system power efficiency.

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References:
[1] M. Lebedev, et al., "Brain-machine interfaces: past, present and future," *Trends Neurosci*, vol. 29, no. 9, pp. 536-546, Sept. 2006.
[2] J. Aziz, et al., "256-Channel Neural Recording and Delta Compression Microsystem with 3-D Electrodes," *IEEE J. Solid-State Circuits*, vol. 44, no. 3, March 2009.
[3] W. Wattanapanitch, et al., "An Engergy-Efficient Micropower Neural Recording Amplifier," *IEEE Trans. BioCAS*, vol. 1, no. 2, June 2007.
[4] R. Harrison, et al., "A Low-Power Integrated Circuit for a Wireless 100-Electrode Neural Recording System," *IEEE J. Solid-State Circuits*, vol. 42, no. 1, Jan. 2007.
[5] Z. Xiao, et al.. "A 20μW Neural Recording Tage with Supply-Current-Modulated AFE in 0.13μm CMOS," *ISSCC Dig. Tech. Papers*, Feb. 2010.
[6] S.O'Driscoll, et al., "A mm-sized implantable power receiver with adaptive link compensation," *ISSCC Dig. Tech. Papers*, Feb. 2009.
[7] S. Venkatraman, et al., "Exploiting the 1/f Structure of Neural Signals for the Design of Integrated Neural Amplifiers," *IEEE EMBS*, Sep. 2009.
[8] M. Staeyaert, et al., "A Micropower Low-Noise Monolithic Instrumentation Amplifier for Medical Purposes," *IEEE J. Solid-State Circuits*, vol. SC-22, no. 6, Dec. 1987.
[9] U. Wismar, et al., "Linearity of bulk-controlled inverter ring VCO in weak and strong inversion," *AICSP*, vol. 5, pp. 59-66, 2007.

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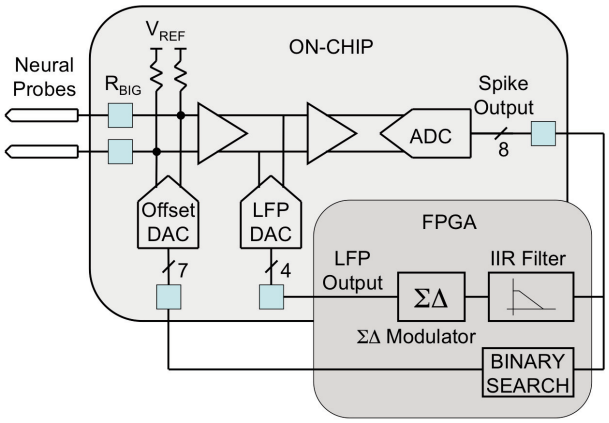

Figure 17.2.1: System block diagram.

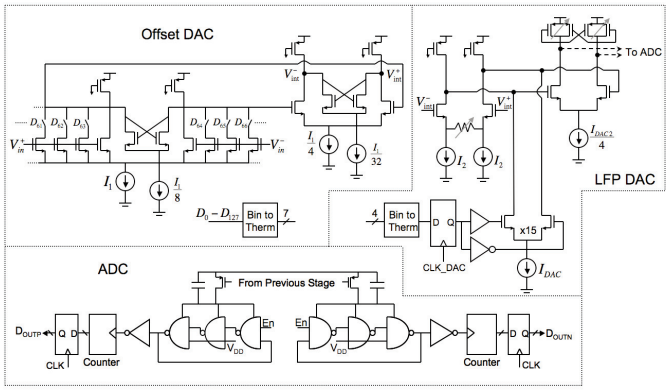

Figure 17.2.2: Circuit schematics.

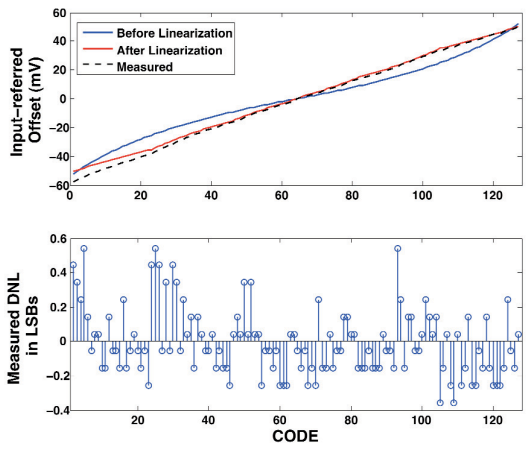

Figure 17.2.3: Simulated and measured offset DAC transfer function and measured DNL. Before linearization uses identically sized elements, while after linearization uses nonlinear coding.

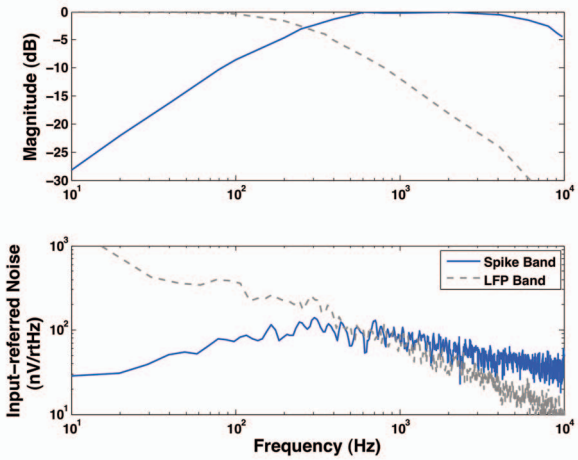

Figure 17.2.4: Measured neural signal acquisition system closed-loop magnitude (above), and Spike and LFP band input-referred noise (below).

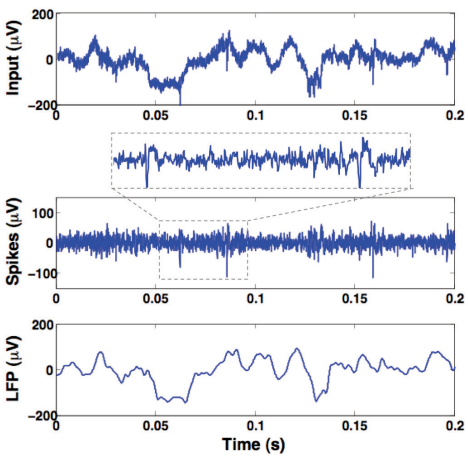

Figure 17.2.5: On-line recordings from the motor cortex of a live awake rat. Top shows complete input waveform before filtering. Middle and bottom show on-chip filtered LFP and Spike outputs.

	Table of Comparisons				
	[2]	[3]	[4]	[5]	This Work
Power (μW)	15	7.56	42.2	0.64	5.04
IRNoise (μV)	7.0	3.06	5.1	14	4.9
Bandwidth	5kHz	5.3kHz	5kHz	6.2kHz	10kHz
NEF	4.6	2.67	9.8	6.5	5.99
NEF^2-VDD	63.48	20	316.9	33.8	17.96
CMRR (dB)	-	66	-	59	75
PSRR (dB)	-	75	-	71	64
V_{DD} (V)	3	2.8	3.3	0.8	0.5
Area (mm^2)	0.04	0.16	0.16	0.4*	0.013
Technology	0.35μm	0.5μm	0.5μm	0.13μm	65nm
Blocks included in comparison	LNA, BPF	LNA, BPF	LNA, BPF	LNA, BPF	LNA, BPF, ADC

*estimated

Figure 17.2.6: Performance summary and comparison with prior art.

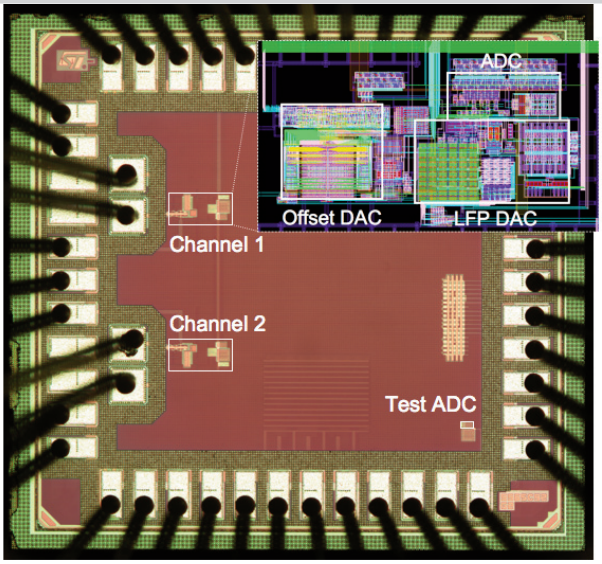

Figure 17.2.7: Die microphotograph; inset shows detailed layout.

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