8.6 A 10b 75ns CMOS Scanning-Display-Driver System for QVGA LCDs

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The display industry is booming as high-performance displays become the main user interface in every mobile device. The current trend toward higher resolution displays means display drivers must be faster, while minimizing power and cost. In order to make displays more appealing to consumers, display manufacturers are also requesting higher driver output swing for higher contrast and better driver accuracy for improved video uniformity.

Recent work has focused on source drivers, where one video channel drives one or two display columns [1]. This source driver architecture eases the speed requirements and capacitive load on the amplifier, but is limited by mismatch in DC offsets between output circuits on the array and between panels. DC errors between columns on a single array lead to vertical stripes that are readily distinguished by the naked eye.

A couple of approaches [2, 3] have been successfully used to reduce DC errors in the video signal, but neither has addressed DC errors in the common (COM) backplane signal. A DC error in COM may result in significant brightness differences between panels in the absence of factory calibration. An additional weakness of the source driver architecture, caused by the high contact resistance of the chip-on-glass (COG) assembly in series with the driver outputs, limits the amplifier output current and ultimately the maximum resolution of the display.

An alternative approach to driving displays consists of using a single high-speed video channel for each color in the display. The main advantage of this high-speed approach is DC uniformity within the display in a significantly smaller die area. The main challenge is the design of a power-efficient amplifier that is capable of providing a high output current to slew the panel's parasitic capacitance and settle in under one pixel clock.

This paper presents a high-speed display driver system fabricated in a standard 0.35μm CMOS technology that operates from a single 3V battery for a 3.0-in. QVGA (320×RGB×240) panel. A new amplifier topology, which provides a slew current 100 times the quiescent current, is discussed. The DAC architecture uses COM as a reference to improve the pixel DC accuracy between different panels.

Figure 8.6.1 shows the system block diagram. A video signal processor takes an 8b serial input and sends 10b words to 3 video channels. Each video channel sequentially drives all pixels of a single color on the display panel. Two 7b DACs and amplifiers drive the common (COM) backplane. Note that the top side of the pixel capacitance is driven by the video channels and the bottom side is driven by the COM channels. A charge pump doubler and low-dropout (LDO) regulator power the analog portion of the system with 5.0V for standard mode, or 5.3V to maximize the video and COM output swing. A high-voltage charge pump provides up to 10V to the panel's level shifters.

The 10b video DAC, illustrated in Fig. 8.6.2, consists of a 6b resistor string followed by a 4b switched-capacitor MDAC [4]. The string DAC passes the voltage above and below the selected resistor element and the MDAC interpolates between these two values. The reset phase of the MDAC, phi1, occurs once per line during the horizontal blanking interval. During this phase, the first stage, A1, is in unity-gain feedback and the amplifier offset is stored on capacitors Cfb and Cdac. The second amplifier stage, A2, is disabled during phi1. Unlike a conventional switched-capacitor circuit, which requires a switch in the signal path, this reset scheme eliminates all switches and their respective parasitics from the signal path.

Since the COM signal can vary depending on the linearity of the COM DAC or offset in the COM amplifier, this novel video DAC architecture resets Cfb to the on-chip COM voltage, *Vcom*. During the sample phase, phi2, A2 is enabled and Cfb provides feedback around stages A1 and A2. The amplifier offset voltage stored during the reset stage is completely cancelled and the video output is now a function of *Vcom*. With the exception of signal-independent charge injection from switch S1, the net voltage across the pixel is now free of DC errors related to the video or COM DACs.

The video amplifier consists of a class A-B input stage followed by a push-pull output buffer, as shown in Fig. 8.6.3. A slew-rate enhanced input stage is used to slew compensation capacitance with a minimal increase in quiescent current and no additional headroom requirement. During quiescent operation, the input stage acts as a class-A differential pair. Amplifier As1 has a built-in offset to ensure transistor M1 is normally off. When there is a large differential voltage across the inputs Vin+ and Vin-, the positive input of As1 follows the higher of the two input signals, while the negative input of As1 follows the lower of the two input signals. When the difference between the two inputs is greater than the offset in As1 the amplifier boosts the gate voltage on the tail current transistor, increasing the current in the stage for the duration of the slewing event. This extra current slews the internal compensation capacitance as well as the input capacitance of the output stage. A2 is implemented as a push-pull stage biased by level-shifting capacitors, which are refreshed at the data rate. The output devices are biased to provide a slew current up to 100 times the quiescent current of the output devices during a slewing condition. The output devices are sized so that the output can swing within 100mV of the rails, resulting in a 0.1 to 5.2V video output swing with a 5.3V power supply.

Figure 8.6.4 shows the step response of the video amplifier. The settling time to 1% accuracy is less than 75ns for a 4V step with a 300pF load. Figure 8.6.5 summarizes the performance of the video channel. Implemented with 0.5μm transistors to achieve a 5V output, the video channel achieves a video-to-COM DC accuracy of <3mV with INL and DNL of 0.4 and 0.1LSB, respectively, in an area of 0.238mm^2. The total video channel current dissipation is 850μA per channel.

The video amplifier performance is compared with recent work [5, 6, 7] in Fig. 8.6.6. The peak current is calculated for each case by multiplying the load capacitance by $0.8 \cdot V_{DD}$ and dividing by ¼ of the settling time. We can then compare the multiplication factor of the peak current to the quiescent current. The >100 current multiplication factor for this work sets a new standard for Class-AB output buffers. A micrograph of the display driver system is shown in Fig. 8.6.7.

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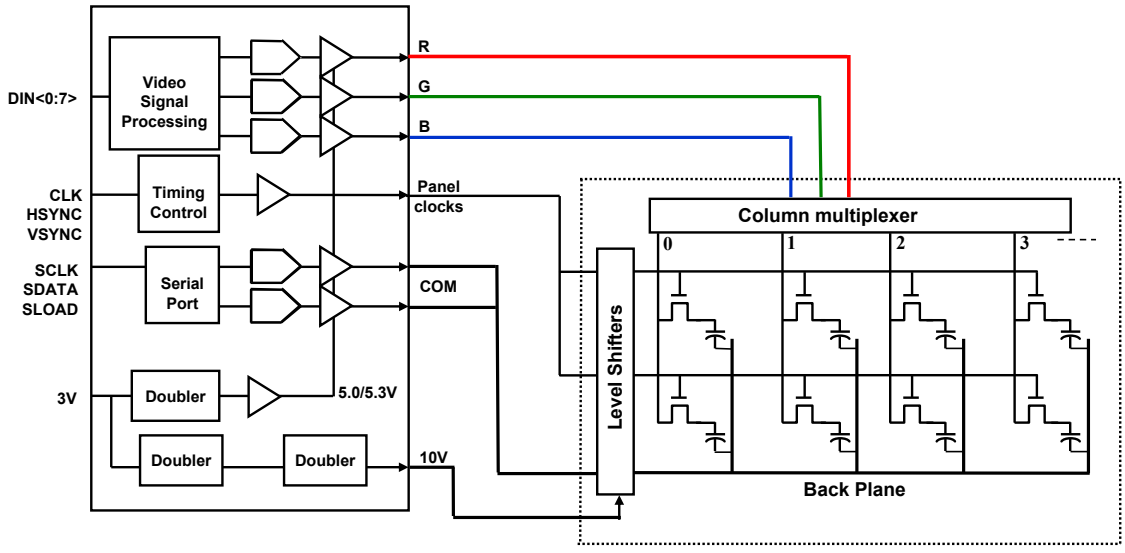

Figure 8.6.1: System block diagram.

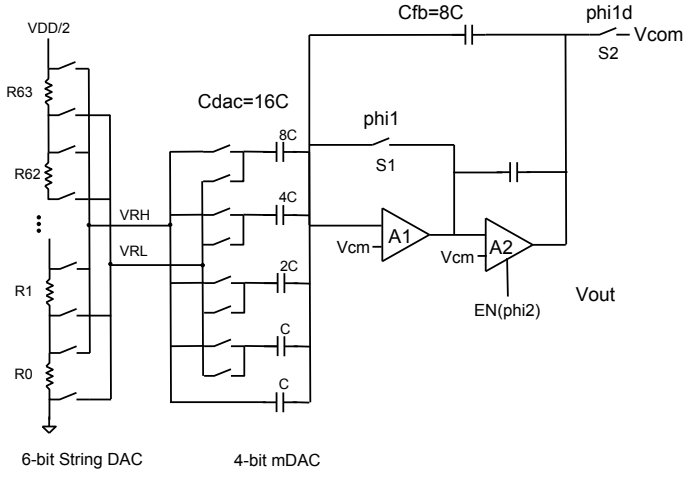

Figure 8.6.2: Segmented video DAC architecture.

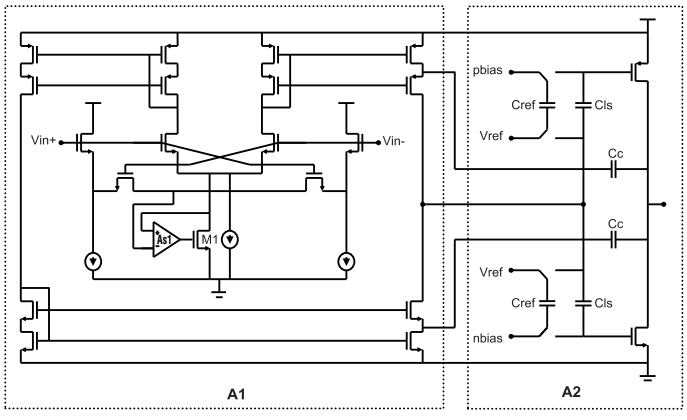

Figure 8.6.3: Video amplifier schematic diagram.

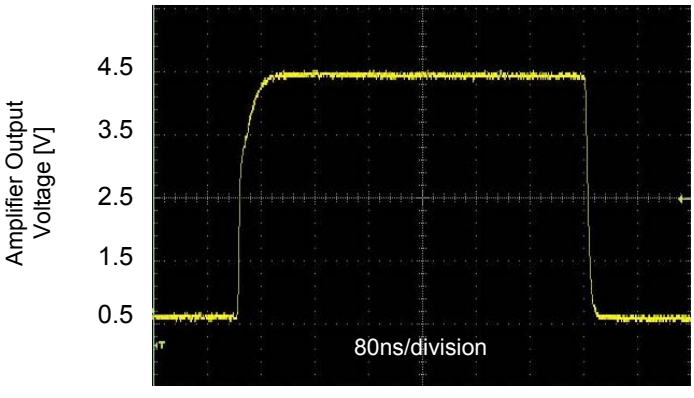

Figure 8.6.4: Video amplifier step response.

Performance Summary		
Application		QVGA LCD display, LTPS backplane
Technology		0.35μm/0.5μm 2P3M CMOS
Video Performance	DAC Resolution	10 bits
	Settling Time	< 75ns for 4V step, 1% accuracy, 300pF load
	Output Swing	0.1V to V_{DD}-0.1V, V_{DD}=5.0V/5.3V
	Quiescent Current	850μA per video channel 600μA for amplifier, 250μA for DAC
	DAC INL/DNL	< 0.4 / 0.1 LSB
	Video to COM DC accuracy	< 3 mV
	Area	0.238 mm² per video channel

Figure 8.6.5: Display driver video channel performance summary.

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	This work	Knausz 2006 [5]	Itakura 2003 [6]	Yu 1999 [7]
Technology	0.5 μm CMOS	0.5 μm CMOS	0.6 μm CMOS	0.8 μm CMOS
VDD [V]	5	5	5	5
Settling time [μs]	0.075	0.450	8.3	8
Cload [pF]	300	300*	30	600
Quiescent current [μA]	600	60	8.2	24
Calculated peak current [mA]	64	2.7	0.058	1.2
Current multiplication factor	107	44	7	50

*Approximate value based on display resolution

Figure 8.6.6: Performance comparison.

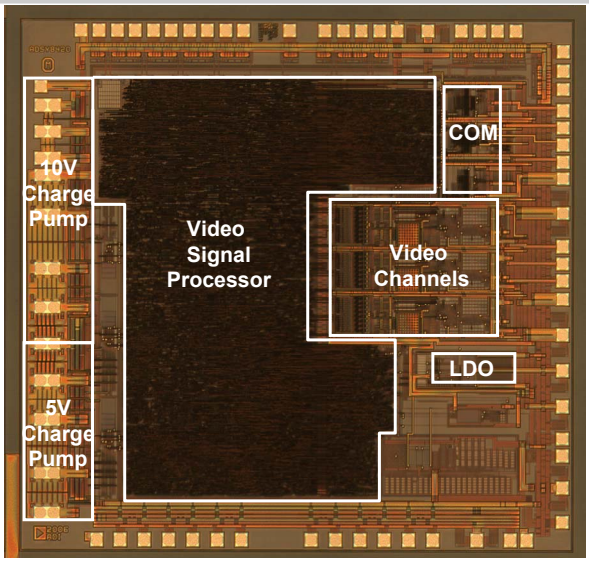

Figure 8.6.6: Micrograph of of the display driver system.

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