A Sub-mm³ Ultrasonic Free-Floating Implant for Multi-Mote Neural Recording

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Abstract—A 0.8-mm³-wireless, ultrasonically powered, freefloating neural recording implant is presented. The device is comprised only of a 0.25-mm² recording integrated circuit (IC) and a single piezoceramic resonator that are used for both power harvesting and data transmission. Uplink data transmission is performed by the analog amplitude modulation of the ultrasound echo. Using a 1.78-MHz main carrier, >35 kb/s/mote equivalent uplink data rate is achieved. A technique to linearize the echo amplitude modulation is introduced, resulting in <1.2% static nonlinearity of the received signal over a \pm 10-mV input range. The IC dissipates 37.7 μ W, while the neural recording front end consumes 4 μ W and achieves a noise floor of 5.3 $\mu V_{\rm rms}$ in a 5-kHz bandwidth. This work improves the sub-mm recording mote depth by $>2.5\times$, resulting in the highest measured depth/volume ratio by $\sim 3x$. Orthogonal subcarrier modulation enables simultaneous operation of multiple implants, using a single-element ultrasound external transducer. Dual-mote simultaneous power-up and data transmission are demonstrated at a rate of 7 kS/s at the depth of 50 mm.

Index Terms—Echo modulation, energy harvesting, implantable biomedical devices, linearization, neural recording, nonlinear acoustics, piezoelectric, ultrasound.

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I. INTRODUCTION

TNTETHERED, wireless neural recording implants are an emerging type of neural interface [1]-[4], which enable improved access to signals valuable for disease diagnosis, closing the loop in stimulation systems, and basic neuroscience research. By their distributed nature, individual wireless devices can precisely target anatomical areas of interest such as deep brain structures or peripheral nerves. Unlike some wireless devices that sit subcranially on the surface of the brain, wireless devices that target deep structures must strictly minimize the size to lessen implantation trauma and long-term tissue scarring [5], which results in signal-quality degradation in chronic neural recording [6]. Reducing device volume to sub-mm³ scales also enables minimally invasive implantation techniques, such as catheter-based, laparoscopic or even injection-based procedures. Designing wireless sub-mm-scale implants with centimeter-deep operation ranges presents power delivery and data transmission challenges. Furthermore, for concurrent recording from multiple sites, the system should also be able to communicate with a network of such implants.

Multiple designs have been reported recently to address the issues outlined above [2]-[4]. The smallest free-floating neural recording implant was presented in [4] whose maximum theoretical operation depth does not exceed 6 mm due to high tissue attenuation, and thus is better suited to the epicortical neural recording. Sequential inductive coupling (using an implanted high-Q tertiary coil) was presented in [3] for transcranial power transmission to epicortical free-floating implants at a depth of 20 mm. This technique cannot be extended to deep tissue recording since the tertiary coil has a large form factor and the implants must be on the same plane (similar to [7], [8]). Recently, uplink data communication with a network of free-floating implants using a random time-division multiple access (TDMA) protocol and a tertiary coil similar to [3] for power transmission was demonstrated in [9]. This implementation is also limited to the epicortical recording due to its shared RF link, the limited operation range (1 cm), and the uplink data rate (10 kb/s/device). A frequencydivision multiple access (FDMA) downlink was proposed in [10] to communicate with an ensemble of sub-mm-scale

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Fig. 1. Untethered neural recording from deep regions of the peripheral/central nervous system using ultrasonically powered neural recording implant.

neural stimulators. This requires the receiving antenna of each implant to be individually designed and tuned at a unique frequency, complicating the design and cost when scaled to multiple motes.

The implant presented in [2] takes advantage of low tissue propagation loss (~0.5 dB/cm/MHz) and low propagation velocity of acoustic waves in realizing a miniaturized, ultrasonically powered implant. However, the absence of a low-noise gain stage limits the SNR of the recorded signal and necessitates the use of a focused ultrasound transducer, restricting the tissue operation depth range to 8.8 mm. Electromagnetically powered implants that are $<1 \text{ mm}^3$ do not meet the depth requirement for recording from the peripheral nervous system (PNS) in human targets such as the Vagus nerve, which is located 3–5 cm below the skin surface [11]. Furthermore, deep-tissue, multi-site neural recording using free-floating implants has not been demonstrated in the aforementioned prior art. A custom-designed beamforming transducer was shown in [12] that can sequentially power up two generalpurpose ultrasonically powered implants. However, due to the continuous operating protocol used in [12], further miniaturization below a mm³ implant volume is challenging, as discussed in the following.

We present the design, implementation, and verification of an ultrasonically powered neural recording implant shown in Fig. 1 [13], which achieves state-of-the-art neural recording performance when compared with other sub-mm³, freefloating wireless implants. The implant occupies a volume of only 0.8 mm³, minimizing tissue displacement, scarring, and foreign body response. The implants have been verified to operate at 50-mm depth in a tissue phantom (with ~0.5-dB/cm attenuation at 2 MHz), enabling recording of most peripheral nerve targets as well as deep brain targets through thinned skull [14]. The implants are designed to enable simultaneous power-up and parallel data back-telemetry of multiple motes with a low-cost single-element unfocused external transducer. This not only simplifies the design of the external interrogator but also maximizes the operation depth and the interrogation frequency (and, hence, the temporal resolution of the acquired signal) in a multi-site recording setup.

The article is organized as follows. In Section II, design requirements and challenges are outlined. The concept of linear analog echo modulation (AM) of an echo for uplink data transmission is introduced in Section III where a theoretical analysis is performed. Section IV describes the circuit-level implementation of the integrated circuit (IC) and measurement results are presented in Section V. Conclusions and comparison with the state-of-the-art are presented in Section VI.

II. SYSTEM OVERVIEW

To miniaturize wireless implants below millimeter scales, the number and size of off-chip components must be minimized. This includes the elimination of off-chip capacitors and necessitates the realization of wireless power and data communication on a single link.

Separate power transmission and data communication links have been demonstrated in ultrasonic implants [15], [16]. This mode of operation, shown in Fig. 2(a), enables continuous data transmission and high data rates, but limits the miniaturization of the implant volume, since it requires two ultrasound resonators preferably tuned at distant frequencies to minimize carrier leakage. A similar implant with a single power-data time-multiplexed piezo was presented in [17] to reduce the implant volume. However, actively driving the piezo increases the number of off-chip components (storage and matching network capacitors) and ultimately its overall size. Alternatively, a single ultrasound link can be used for both power and uplink data transmission in a pulse-echo fashion [2], obviating the need for any secondary resonator or off-chip capacitor. In this scheme, shown in Fig. 2(b), an ultrasound pulse is first launched toward the implant. After a single time of flight, the implant ultrasound resonator, realized by a bulk piezoceramic (Lead Zirconate Titanate, PZT), starts resonating and harvesting energy. Shortly after that, the IC on the implant wakes up and begins recording neural signals. At the same time, the amplitude of the echo (traveling toward the external transducer) is modulated according to the recorded neural signal. The AM-modulated echo is then received and reconstructed through the same external transducer. This pulse-echo interleaved scheme prevents overlapping of the high-voltage signals (up to 30 V_{peak}) driving the external transducer and the mV-level received echo signals, which would otherwise impose an impractically large dynamic range (e.g., 110 dB and 30-V input range) on the external receiver front end.

To minimize the number of off-chip components and the overall implant volume, a pulse-echo interleaved scheme similar to [2] is used in this work, with three key differences.

- 1) The addition of a low-noise analog front end (AFE) in this work reduces the input-referred noise by $34 \times$.
- The introduction of a technique to linearize the reflection coefficient, resulting in linear analog amplitude modulation of the echo and, thereby, lowering distortion, as discussed in Section III.
- 3) Simultaneous multi-implant interrogation is achieved without sacrificing the interrogation frequency and with the use of a single-element external transducer.



Fig. 2. Various ultrasound operating protocols. (a) Continuous-mode operation where on-off keying (OOK) is used for uplink data transmission. (b) Pulse-echo mode with classic AM uplink data transmission. (c) Pulse-echo mode with simultaneous interrogation of two implants using orthogonally encoded AM.

Both focal length (Fresnel distance) and focal area of an ultrasound transducer scale with its aperture. For instance, a low cost commercially available single-element 0.5" diameter unfocused external transducer has a focal length of 52 mm and focal area of 50 mm² at 2 MHz in water. Therefore, we propose a network of sub-mm-scale implants scattered over this 50-mm² focal area that simultaneously power up and perform data back-telemetry. For uplink data transmission, each implant has a unique orthogonal subcarrier that utilizes code-division multiplexing (CDM), while modulating the amplitude of its echo. In this prototype, the chip internally generates a CDM code by dividing the clock (extracted from the main carrier) by a ripple counter. In a multi-implant setup, CDM codes can be generated in the same fashion [18]; a frequency divider is clocked by the extracted global main carrier and followed by an encoder to generate CDM codes. A unique code may be chosen by trimming or hardwiring the device. The encoded echoes from multiple implants are superimposed in the acoustic medium and received by the external transducer, as shown in Fig. 2(c). The receive chain of the interrogator includes a low-noise amplifier (LNA) and a high-resolution ADC. Decoding an echo is only a matter of synchronized code multiplication and averaging. Upon echo and CDM code multiplication at the receiver, the signal associated with the CDM code is converted into baseband while those of the other channels will remain spread across the spectrum. Averaging concurrently generates a single sample of the selected channel and filters out the non-selected channels. Decoding is possible regardless of the length of the encoded echo as long as it contains an instance of a CDM frame. This is crucial because the duration of the time-interleaved echoes is finite (and often short, approximately tens of microseconds). In addition, orthogonal codes can serve as a subcarrier signal



Fig. 3. Top: Typical ultrasound pulse with AM. Bottom: Comparison between analog and DM schemes and their corresponding bounce diagrams.

that partially bypasses the low-frequency noise contents of the main carrier [19].

Fig. 3 shows a typical echo pulse of the implant when AM is used for data back-telemetry. After implant powerup and initialization, the amplitude of the echo is modulated according to the recorded neural signal. A comparison between the required echo period $T_{echo,min}$ for analog and digital echo modulation (DM) along with their bounce diagrams are shown in Fig. 3. Assuming the same number of ultrasound cycles $(1/f_{main,carrier})$ is required for the ampli-



Fig. 4. Simplified block diagram of the IC.

tude to settle or switch between states, the required pulse period for the case of DM is larger than that of AM by roughly the number of digital bits transmitted in each echo. In other words, AM carries higher information per cycle than DM. To prevent overlapping the transmitted pulse and the echo, the pulse duration must be smaller than the round-trip time between the external interrogator (Tx) and the implant (Rx), or <2ToF. Thus, the minimum distance between the implant and the external transducer in the case of B-bit digital modulation, $d_{\min,DM}$, is B times larger than that of AM. For a $d_{\min,AM}$ distance shown in Fig. 3, only a single bit of data can be transmitted using DM. The same principle holds true when subcarrier modulation takes place. The maximum interrogation frequency in a pulse-echo communication channel is given by $f_{\text{sample}} = 1/2T_{\text{echo,min}}$. In addition to extending the operating range (by allowing shorter distances between Tx and Rx), AM uplink requires shorter $T_{echo,min}$ and, hence, can enable higher interrogation frequencies and ultimately uplink data rates.

A simplified block diagram of the implant is shown in Fig. 4. The chip contains a power management block that rectifies and regulates the received piezoceramic (piezo) voltage to a 1-V supply. A clock signal is directly extracted from the piezo-harvested voltage (using 2.5-V buffers), which is divided to generate the chopper signal. The AFE consists of a fully differential chopper-stabilized amplifier followed by a linear gm-cell that linearly modulates the amplitude of the echo. After receiving and conditioning the echo at the external interrogator, digital post-processing, shown in Fig. 2(c), is performed to reconstruct the transmitted signal. The implant is powered on as long as an ultrasound pulse is present, meaning that the implant is memoryless. This hinders electrode dc offset cancellation. Therefore, the inputoutput linear range of the implant should be extended to minimize distortion. The input linear range of the implant is beyond ± 10 mV. The output (echo) modulation linearity is achieved by linearly modulating the piezo voltage, as discussed in Section IV.



Fig. 5. (a) Echo amplitude modulation distortion caused by Γ - R_E nonlinearity. (b) Piezo equivalent circuit at f_s .

III. LINEAR ECHO MODULATION

The profile of the acoustic reflection coefficient Γ of a piezo as a function of its termination resistance R_E is shown in Fig. 5(a). It can be observed that the modulated echo is significantly distorted due to the nonlinearity of Γ , especially when concurrent energy harvesting with echo modulation imposes a minimum value of termination resistance $R_E = R_{\min}$. That is, R_{\min} should be large enough to allow energy harvesting. This is not a typical problem for digital modulation when transmission of only two states is needed. For AM modulation, however, the source of this nonlinearity should be understood and, if possible, linearized through co-design of the piezo and the modulating IC. However, the governing equations of bulk piezos as well as their equivalent circuit models (KLM [20] and Redwood [21]) are complex and provide little insight into the source of this nonlinearity. Instead, analytical derivation and experimental verification of a simple expression can guide the modulator design and lead to linear echo modulation received at the external interrogator. Such an expression is introduced in this section and used in Section IV to implement a linear echo amplitude modulator.

The piezo is modeled as a thickness-mode resonating threeport network, shown in Fig. 6(a), whose input–output port relationships are well described by [22]

$$\begin{bmatrix} F_1 \\ F_2 \\ V_3 \end{bmatrix} = \mathbf{P} \begin{bmatrix} v_1 \\ v_2 \\ I_3 \end{bmatrix} = \begin{bmatrix} m & n & p \\ n & m & p \\ p & p & r \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ I_3 \end{bmatrix}$$
(1)

$$\begin{bmatrix} F_1\\F_2\\V_3 \end{bmatrix} = \begin{bmatrix} \frac{Z_0A}{j\tan(\beta l)} & \frac{Z_0A}{j\sin(\beta l)} & \frac{h_{33}}{j\omega} \\ \frac{Z_0A}{j\sin(\beta l)} & \frac{Z_0A}{j\tan(\beta l)} & \frac{h_{33}}{j\omega} \\ \frac{h_{33}}{j\omega} & \frac{h_{33}}{j\omega} & \frac{1}{j\omega C_0} \end{bmatrix} \begin{bmatrix} \nu_1\\\nu_2\\I_3 \end{bmatrix}$$
(2)

Ports 1 and 2 are acoustical, and Port 3 is the electrical port of the piezo. Table 1 describes the parameters used in (2). The acoustic impedance seen into Port 1, while Port 2 and 3 are, respectively, terminated by Z_B and Z_E [Fig. 6(b)], is given by

$$Z_1 = \frac{p^2(2n - 2m - Z_B) + (Z_E + r)(m^2 - n^2 + mZ_B)}{(Z_E + r)(m + Z_B) - p^2}.$$
 (3)

Therefore, Γ is given by

$$\Gamma = \frac{Z_1 - Z_B}{Z_1 + Z_B}.$$
(4)



Fig. 6. (a) Piezo resonator modeled by a three-port network defined by matrix **P**. (b) Z_1 is the acoustical impedance seen into Port 1, while Port 2 is terminated by tissue acoustic impedance Z_B and Port 3 is terminated by Z_E . (c) Z_3 is the electrical impedance seen into Port 3, while the acoustical terminals are terminated by Z_B . (d) $Z_{3,\text{NL}}$ is the unloaded electrical impedance of the piezo.

TABLE I LIST OF PIEZOELECTRIC TYPICAL PARAMETERS

Parameter	Unit	Value	Description	
ρ	kg.m ⁻³	7600	Piezo Density	
ϵ_{33}	$\rm nF.m^{-1}$	16.8	Piezo Dielectric constant	
c_{33}^{E}	GPa	50	Piezo Elastic constant	
$c_{33}^{\tilde{D}} = c_{33}^{E}(1+k^{2})$	GPa	73	Stiffened c_{33}	
e_{33}	$\rm C.m^{-2}$	20	Piezo Stress constant	
$h_{33} = e_{33}/\epsilon_{33}$	$GC.m^{-1}.F^{-1}$	1.18	Piezo constant	
$k = e_{33} / \sqrt{\epsilon_{33} \cdot c_{33}^E}$	_	0.69	Electromechanical coupling	
$k_t = \sqrt{k^2/(1+k^2)}$	_	0.56	_	
$v_a = \sqrt{c_{33}^E/\rho}$	${ m m.s^{-1}}$	2564	Piezo wave velocity	
$\overline{v_a} = v_a \sqrt{1 + k^2}$	$\mathrm{m.s}^{-1}$	3115	Stiffened v_a	
A	mm^2	0.56	Piezo cross-section area	
$C_o = A\epsilon_{33}/t$	$_{\rm pF}$	12.6	Piezo capacitance	
$Z_o = \rho \overline{v_a}$	$MPa.s.m^{-1}$	23	Piezo acoustic impedance	
$f_p = \frac{1}{2}\overline{v_a}/t$	MHz	2.07	Parallel resonance frequency	
$\bar{f_s} = \bar{f}p/\sqrt{1+8(k/\pi)^2}$	MHz	1.76	Series resonance frequency	
$\beta = 2\pi f / \overline{v_a}$	m^{-1}	_	wave propagation constant	

It is shown in the Appendix that at the series resonance frequency of the piezo, (4) further simplifies to

 $\Gamma \approx rac{Z_E}{Z_E + R_S} \propto V_3$

$$R_{S} = \frac{2Z_{B}p^{2}}{(n+m)^{2}} = 2Z_{B}\left(\frac{mr-p^{2}}{m^{2}-n^{2}}\right)$$
(6)

is the internal series resistance of the piezo. At f_s , Γ is approximately linearly proportional to the voltage across Port 3 (coupling the simplified circuit model of Fig. 5(b) to the acoustical port of the piezo). Therefore, to linearly modulate Γ , the voltage across the piezo should be linearly modulated. Fig. 7 compares the analytical expression (4) and its approximation (5) for the parameter values listed in Table 1, showing excellent matching between the expressions and the measured values. In contrast to (4), (5) has a single parameter, R_S , which can be obtained empirically or by finite-element model (FEM) simulation. To verify the model, measurements were made on a $0.75 \times 0.75 \times 0.75 \text{ mm}^3$ piezo (854, APC International), whose $R_S = 1.5 \text{ k}\Omega$.

IV. INTEGRATED CIRCUIT IMPLEMENTATION

The implemented mote utilizes a $0.75 \times 0.75 \times 0.75$ mm³ piezo (840, APC International), whose $R_S = 4$ k Ω . When



Fig. 7. Normalized Γ - R_E curve obtained by (4), (5), and measurement.



Fig. 8. (a) Schematic of power management blocks. (b) Chip-level timing diagram shown with two subcarrier cycles.

an ultrasound pulse is received at the piezo, the IC has a finite amount of time (< 2ToF, e.g., 66 μ s at 50-mm depth) to power up, generate a stable supply, record neural signals, and perform uplink data transmission. Therefore, rapid powerup and precise timing management of the sub-blocks are critical. The interconnection of power management blocks and the top-level timing diagram of the chip are shown in Fig. 8. Due to the time constant associated with the onchip storage capacitor (130 pF), the internal series resistance of the piezo, and the $< 2\pi$ conduction angle of the rectifier, it takes $\sim 5 \ \mu s$ (approximately ten ultrasound cycles) to fully charge up the storage capacitor and for the supply-independent proportional-to-absolute-temperature (PTAT) source to generate two reference voltages ($V_{ref,1V}$ and $V_{ref,0.5V}$) on-chip. The PTAT core transistors M_{1-4} are designed to operate in the subthreshold region such that $I_{M5} = \eta V_T \text{Ln}(W_2/W_1)/R_{\text{ref}}$

(5)



Fig. 9. LNA topology and timing diagram.

where η and V_T are the subthreshold factor and the thermal voltage, respectively. Initially, M1-8 are off and the gates of M_{7-8} track V_{rect} . Upon harvesting voltage from the piezo, V_{rect} rises, and M_{7-8} turn on pulling up/down the gates of M_{1-2}/M_{3-4} to speed up their transition from zero current to the desired current (500 nA) stable bias point. M₆ is designed to be strong enough to pull down the gates of M_{7-8} , charging C_{start} and disengaging the PTAT startup circuitry once M_{1-2} turn on. $V_{ref,1V}$ serves as the low dropout regulator (LDO) reference voltage, and a delayed version of $V_{ref,1V}$ triggers the power on reset (POR) to initialize the logic states. The amplifier initialization takes 3 μ s, which is followed by signal acquisition and uplink data transmission. In the absence of an ultrasound pulse, the on-chip storage capacitor discharges in $\sim 10 \ \mu$ s, meaning that inter-pulse duration should be greater than 10 μ s for proper re-initialization (POR triggering) of the IC. This translates to a minimum operation depth of 14 mm without requiring any acoustic spacer.

A. Low-Noise Amplifier

The AFE of the chip consists of a fully differential capacitive-feedback LNA whose circuit diagram is shown in Fig. 9. The values of the feedback and load capacitors (0.44 and 4.7 pF, respectively), and the feedback factor ($\beta \sim 1/16$) set the noise ($< 10 \mu V_{\rm rms}$ in 180-kHz bandwidth) of the circuit, while the effective transconductance of the LNA sets the bandwidth. The amplifier is initialized by a set of switches controlled by ϕ_{1-4} , which bias the LNA as quickly as possible to maximize the signal acquisition period. $V_{\rm CM}$ is set to the 0.5-V mid-rail voltage using a power-gated linear regulator shown in Fig. 10. The low-impedance source charges 25 pF of capacitance in $< 1 \mu$ s.



Fig. 10. (a) Fully complimentary OTA topology used in the LNA. (b) Powergated charger of the input terminals of the OTA.

Since the LNA runs on a 1-V supply and has a gain of 16, auto-zeroing is implemented to cancel the amplifier offset and improve the linear output voltage swing [23]. Auto-zeroing is implemented by sampling the offset of the amplifier on the feedback capacitors (C_f). The ϕ_1 switches are disabled first, placing the amplifier in the unity gain feedback. The sampled offset is then subtracted from the signal after sequentially opening ϕ_2 and ϕ_3 and establishing the signal path through ϕ_4 . The sequential switching results in the kT/C noise that is added to the sample after the initialization period of each interrogation event. To mitigate kT/C noise, the input signal is chopper-stabilized and upmodulated to a frequency f_{chop} , while the kT/C noise remains at baseband. When the signal is downmodulated, the kT/C noise is converted into out-ofband chopper ripple [24]. Since downmodulation occurs on the interrogator side, chopper stabilization is used to simultaneously bypass the 1/f and kT/C noises of the amplifying circuits as well as the low-frequency noise contents of the main carrier. In the presence of chopping switches, the input impedance of the amplifier is given by $Z_{in} = 1/(2f_{chop}C_s) \sim$ 1.3 M Ω at the highest chopping frequency of 55 kHz. The impedance of the electrodes submerged in saline was measured to be an order of magnitude smaller than the input impedance of the AFE ($\sim < 100 \text{ k}\Omega$) for frequencies greater than 100 Hz (Fig. 14).

The total output-referred noise power of the amplifier is given by $\overline{v_n^2} = kT\alpha\gamma/(\beta C_T)$ [25], where k is the Boltzmann constant, T is the absolute temperature, α is the excess noise factor of the operational transconductance amplifier (OTA), γ is the MOS channel noise coefficient, and C_T is the total capacitance seen at the output node during amplification. The bandwidth of the LNA is given by $\omega_{3dB} = \beta G_m / C_T$, where G_m is the effective transconductance of the OTA. A fully complementary differential amplifier topology [26] shown in Fig. 10(a) is chosen, since its α is close to 1, and it has a high G_m/I_D , since $G_m = g_{m,N} + g_{m,P}$. The output range of the LNA is ± 160 mV, with a bandwidth of 180 kHz, high enough to pass the third harmonic of the highest subcarrier frequency (55 kHz). Although the amplifier has a broadband forward path of 180 kHz, the bandwidth of the post-processed signal and, therefore, the effective noise



Fig. 11. Linear gm-cell architecture.

bandwidth of the amplifier are reduced to 5 kHz at an interrogation frequency of 10 kHz. Along the signal chain, as shown in Fig. 2(c), decoding and demodulation of the echo involve averaging the echo for the duration of the pulse. This averaging concurrently applies a sinc low-pass filter with a 3-dB bandwidth of $1/2T_{\text{integration}}$ to the received signal and translates every received echo to a single sample. Therefore, at a 10-kHz interrogation frequency (sampling frequency), the signal and noise bandwidth are reduced to 5 kHz. At last, the auto-zeroing noise foldover does not degrade the noise performance of the front end for the amplifier is already a sampled one where the input-referred sampled thermal noise voltage of the broadband amplifier during the amplification phase is almost $6 \times$ larger than that sampled and translated to baseband during the auto-zero phase. This is due to β and C_T being $16 \times$ and $2.5 \times$ larger, respectively, during the auto-zero phase than those during the amplification phase.

B. Linear G_m -Cell Design

The LNA drives a linear transconductance stage for converting the acquired signal to current. The G_m -cell, therefore, requires a ± 160 -mV input voltage range with better than 0.5% nonlinearity. This is achieved by forcing the input voltage across a PFET device biased in the triode region with a differential super source follower (Fig. 11) [27]. A PFET device is used instead of a resistor to save area without sacrificing linearity. A Δ incremental increase of V_{in} results in both $|V_{DS}|$ and $|V_{GS}|$ of M_M to increase by, respectively, Δ and $\Delta/2$, which gives rise to $I_{M_M} \propto \Delta$ as long as M_M is in triode region, which is ensured by designing M_M as a longchannel low-Vt device. The current generated through M_M creates a pair of differential current signals passing through M_1 and M_2 , which is converted into single-ended in the last stage of the G_m -cell. The G_m stage has a nominal transconductance of 120 μ S. The 1-V supply powers this stage, except for the final current mirror, which is connected directly to the rectifier output and provides the signal for uplink data modulation; 2.5-V devices are used in the final mirror stage due to higher rectifier voltages.

C. Linear Echo Modulator

The linear relationship between Γ and V_3 , expressed in (5), reveals that linear amplitude modulation of the echo is possible 3023



(a) Conceptual echo amplitude modulation using synchronous up-Fig. 12. conversion current mixer. (b) Reusing active rectifier as synchronous mixer. (c) Nonlinearity induced by the rectifying modulator.

by linearly modulating the amplitude of the piezo voltage $(V_{PZ} = V_{PZ}^+ - V_{PZ}^-$ in Fig. 12). At resonance, the piezo is modeled by an ac voltage source (V_s) and the series resistance of the piezo (R_s) . Consider the conceptual circuit diagram shown in Fig. 12(a) where it is assumed the signal modulating the echo amplitude is available in the current domain, I_m . To modulate the amplitude of the piezo voltage, I_m is upmodulated by a current mixer whose switching phase is synchronous to the piezo voltage. This results in the peaks and valleys of the piezo voltage dropping by $I_m R_s$. A similar AM modulation technique holds true for reflective antenna systems.

In this work, the synchronized up-conversion current mixer is implemented with minimal hardware overhead by reusing the active rectifier. The circuit diagram of the active rectifier is shown in Fig. 12(b), where high-frequency common-gate RF amplifiers are used as comparators. Since the rectifiers are inherently nonlinear, rectifier-induced nonlinearity should be taken into account. It can be shown that the relationship between the dc voltage at the output of the rectifier V_{rect} and the load current I_m is given by

$$I_m \propto \frac{V_s}{R_s} (1 - \frac{V_{\text{rect}}}{V_s}) \left(1 - \frac{2}{\pi} \operatorname{asin}\left(\frac{V_{\text{rect}}}{V_s}\right) \right)$$
(7)

where V_s is the peak value of the piezo open-circuit voltage. Equation (7) is shown in Fig. 12(c), where the nonlinearity between V_{rect} (normalized to V_s) and I_m (normalized to V_s/R_s) is shown for 10% modulation depth. The voltage across the piezo (V_{PZ}) is the upmodulated version of V_{rect} ; therefore, V_{rect} and V_{PZ} voltages are equivalent in (7). For 10% modulation depth, the maximum nonlinearity between V_{PZ} (and ultimately Γ) and I_m is less than 0.5%. Since rectifier nonlinearity was shown to be minimal, a singleended Gm-cell was connected to the output of the rectifier, mitigating the need for the Gm-cell to sink current from both



Fig. 13. (a) Fully packaged implant micrograph. (b) IC micrograph. (c) Dimensions of the fully packaged implant. (d) Power consumption breakdown.



Fig. 14. Measured ENIG electrode impedance (mean of measurements for six electrode pairs). Inset: single-electrode model.

terminals of the piezo to maintain the full conduction angle if connected to the input of the rectifier.

V. MEASUREMENT RESULTS

The IC was fabricated in the TSMC 65-nm LP CMOS process. The die micrograph and the fully assembled implant are shown in Fig. 13. The bulk piezo and the chip are bonded to a flex PCB interposer. A pair of $200 \times 200 \ \mu m^2$ electroless nickel immersion gold plated electrodes (ENIG) are designed on the backside of the PCB with 2-mm spacing. The measured impedance of the ENIG electrodes (mean of measurements for six electrode pairs, measurements made using a precision LCR meter, Keysight E4980A) submerged in phosphate-buffered saline (PBS $1 \times$) and a model for a single electrode are shown in Fig. 14. The maximum measured (24-h post submersion) electrode dc offset was 1.1 ± 0.4 mV. The implant is encapsulated with $\sim 10 \ \mu m$ of Parylene-C [28]. The total area of the chip, including test pads and on-chip decoupling capacitors, is 0.25 mm². The minimum voltage amplitude required at V_{rect} was measured to be 1.25 V. The circuit power dissipation after rectification was $\sim 30 \ \mu$ W, and the total power consumption including the efficiency of the power management circuits was



Fig. 15. (a) Benchtop measurement setup. (b) Single-mote *in vitro* measurement setup.

measured to be 37.7 μ W during normal operation with a 50% duty cycle. The breakdown of the power consumption is shown in Fig. 13(d).

The chip characterization setup and measurement results are shown in Figs. 15-18. The setup includes a piezo model, an ac-coupled voltage source in series with a 4-k Ω resistor, connected to the piezo terminals of the chip. The output was measured using a fully differential lock-in amplifier for maincarrier demodulation. Subsequent signal processing steps, e.g., subcarrier demodulation, were performed on a PC. The output transient response of the chip, measured at the piezo voltage terminals, is shown in Fig. 16(a) in response to a 20-mV_{PP} input sine wave for five consecutive interrogation events. The first interrogation event is shown in Fig. 16(b) where 11 μ s of power-on/startup time and the 27.5-kHz subcarrier signal are observable. The demodulated and reconstructed input signal for the same measurement is shown in Fig. 16(c). Static and dynamic nonlinearity measurement results are shown in Fig. 17. An end-to-end voltage gain $(\Delta V_{PZ}/v_{in})$ of 23 dB with a maximum static non-linearity error of 1.2% was measured. The power spectrum of the reconstructed 313-Hz, 20-mV_{PP} sine wave is shown in Fig. 17(b) and achieved an spurious-free dynamic range (SFDR) of 50 dB and a THD of -44 dB. No harmonic tones are visible for a 10-mV_{PP} input signal.

The noise measurement results are summarized in Fig. 18 for an interrogation (sample) frequency of 10 kHz. There are two major contributors to the total input-referred noise density: the AM noise of the carrier and the noise contributed by the recording circuits. The total input-referred noise spectral density was measured to be 328 nV/ \sqrt{Hz} . This is mainly dominated by the carrier noise, measured at 319 nV/ \sqrt{Hz} in the absence of the chip [Fig. 18(a)]. Both the curves in Fig. 18(a) are derived by down-chopping and averaging, which partially removes the 1/f noise of the carrier. Assuming the noise of the carrier and that of the chip are additive, the input-referred noise of the chip alone can be estimated to be 76 nV/ $\sqrt{\text{Hz}}$ or 5.37 μV_{rms} in a 5-kHz bandwidth. The effect of chopping in bypassing the low-frequency noise contents of the main carrier is demonstrated in Fig. 18(b), where 1/f noise is clearly visible in the spectrum when chopping is disabled.

The single-mote *in vitro* measurement setup is shown in Fig. 15(b), where a single assembled mote is suspended at a distance of 45–60 mm away from a single-element external transducer in oil (with \sim 0.5 dB/cm attenuation at 2 MHz).



Fig. 16. Benchtop measurement result showing amplitude modulation of the input voltage of the rectifier. (a) Five consecutive sample pulses for a 313-Hz, 20-mV_{PP} input signal. (b) First interrogation event where startup time and the subcarrier signal are visible. (c) Demodulated input-referred signal.



Fig. 17. (a) Static input–output (defined as the input voltage of the rectifier) linearity curve of the chip. (b) Power spectral density of the reconstructed signal shown in Fig. 16.

The implant was interrogated at 8 kS/s. The main carrier frequency was set to the resonant frequency of the implant piezo at 1.78 MHz. A subcarrier frequency of 55 kHz was generated on chip. Two received sample echoes that form a peak and valley of a 313-Hz, 20-mV_{PP} signal are shown in Fig. 19 along with their demodulated signals. The reconstructed received signal and its spectrum are also shown in Fig. 19(e) and (f). Although the noise of the carrier (generated by the external ultrasound pulser) dominates the overall noise of the link, for the 20-mV_{PP} input range of the implant, 47.96 dB of SNR is measured. Were the carrier noise absent, the SNR would improve by $\sim 10-12$ dB. Fig. 19(g) summarizes the measured SNR and the equivalent uplink data rate measured at multiple other possible configurations with varied depths, interrogation frequencies, and subcarrier frequencies using the same setup introduced earlier.

To make sure an even number of subcarrier cycles [e.g., two in Fig. 19(d)] are used for demodulation, first, echo duration is chosen to be sufficiently long. For instance, >29 and >47 μ s echoes are needed for two and four cycles of a 55-kHz sub carrier, respectively. Since the startup time



Fig. 18. Noise measurement. (a) Noise spectral density of the carrier alone and that obtained from the chip: noise is dominated by the carrier noise. (b) Effect of chopping in reducing the low-frequency noise contents of the main carrier.

and, consequently, the start of the echo modulation period of the chip are consistent from sample to sample, and since the period of the sub carrier is known and referenced to the main carrier frequency (e.g., 1.78 MHz \div 32 = 55 kHz), the subcarrier signal can be determined at the interrogator receiver for demodulation. For pulses longer than the ones mentioned above (29 and 47 μ s), the received echoes are truncated to 29 μ s and 47 μ s such that only an even number of cycles are used for demodulation.

Further *in vitro* verification of the mote was performed where an 800-ms stream of pre-recorded neural signal (acquired by Plexon multichannel acquisition processor) from an awake-behaving rat (Long–Evans) motor cortex was fed to the chip and wirelessly transmitted to the external interrogator. The mote was placed at the depth of 45 mm in a tissue phantom (with ~0.5 dB/cm attenuation at 2 MHz) and interrogated at 10 kS/s. Fig. 20 shows the comparison between the reference pre-recorded neural signal with the signal recorded and wirelessly transmitted by the mote.



Fig. 19. Single-mote *in vitro* measurement results. Implant is interrogated at 8 kS/s at 5-cm depth. (a) and (b) Two received echo signals each translating into a sample shown in (e). (c) Their corresponding AM demodulation. (d) Common-mode rejection of received echoes. (e) Reconstructed 313-Hz signal. (f) SNR of received signal (noise dominated by carrier noise). (g) Measured SNR and equivalent uplink data rate versus input range of the implant.

The effects of misalignment on the operating range of the device were characterized. Fig. 21 outlines a set of measurement results reporting the harvested piezo voltage and the maximum modulation depth of the echo at various relative locations of the external transducer and the implant piezo. The measurement medium was oil with ~ 0.5 dB/cm attenuation at 2 MHz. An unfocused 0.5" diameter external transducer was driven at 1.78 MHz by a ± 15 -V pulser. The maximum modulation depth is defined based on the received echo amplitude at two extreme piezo terminations, open- and short-circuited piezos. Fig. 21(a) illustrates that the harvested power is maximized at the Fresnel distance of the external transducer (~ 52 mm) and that the optimal operation depth of the implants is ~ 50 mm where the harvested voltage and the modulation depth are concurrently large. Moreover, at 70 mm of depth, acceptable harvested voltages (> 4.5 Vpp) and maximum modulation depth greater than 20% were measured. It is also observed that beyond the Fresnel distance, the modulation depth steadily decays at a rate of 6% per cm, allowing a large range of viable implant depths for the mote. Fig. 21(b) and (c) demonstrates similar measurement results for horizontal x- and y-axis misalignment between the implant piezo and the external transducer. It can be observed that the effect of horizontal misalignment is symmetric with respect to the line of sight (LoS); a slight asymmetry in Fig. 21(c) is due to the setup, which includes a rod holding the piezo along the x-axis. Since the chip is fully operational at harvested voltages greater than 4.2 Vpp, horizontal misalignment of up to ± 1.75 mm is acceptable at a cost of a negligible drop in the modulation depth. The ± 1.75 mm misalignment margin is directly proportional to the aperture of the external transducer; therefore, the margin can be doubled by using a 1'' external transducer.



Fig. 20. (a) 800-ms stream of pre-recorded neural signal recorded (at 10 kS/s) and wirelessly transmitted by the mote at 45 mm of depth. Comparison of reconstructed data between (b) single and (c) multiple action potential events.

Fig. 22 demonstrates an *in vitro* measurement setup where two implants at a depth of 50 mm with a 2 mm separation were synchronously powered up by a single 0.5" unfocused external transducer. The setup environment limits the depth in this dual-mote measurement. The subcarrier frequencies of the implants are orthogonal to each other (55 and 27.5 kHz) to enable simultaneous uplink data transmission in this dual-mote setup. Each implant transmitted a single tone (414 and 313 Hz) to the external receiver. The reconstructed tones are shown in Fig. 22(b) along with their spectra. Measured signal-to-noise-and-distortion ratio (SNDR) and SFDR are shown as a function of vertical



Fig. 21. Measured piezo-interrogator relative misalignment characterization in (a) vertical and (b) horizontal y-axis and (c) horizontal x-axis dimensions.



Fig. 22. Simultaneous power-up and data transmission of two implants at a depth of 50 mm and a separation of 2 mm. (a) *In vitro* measurement setup. (b) Reconstructed signals at the external interrogator. (c) and (d) Spectra of the reconstructed signals. (e) and (f) Measured SNDR and SFDR of each channel versus vertical misalignment between the motes.

misalignment between motes in Fig. 22(e) and (f), respectively. It can be observed that the uplink data transmission quality is maintained over ± 2 mm of vertical misalignment. A given vertical misalignment ΔZ between two implants results in the implants powering up with a delay equal to $\Delta t = \Delta Z/c$, where c is the propagation speed of sound in tissue. This delay, in turn, results in subcarriers becoming out of phase by Δt , which translates to inter-channel crosstalk and, consequently, degradation of SNDR and SFDR. Given the carrier frequency and the highest frequency of the orthogonal codes are 1.78 MHz and 55 kHz, respectively, at depths between 35 and 70 mm, four implants can be simultaneously interrogated.

VI. CONCLUSION

We present a 0.8-mm³ free-floating implant that uses a single ultrasound link for wireless power harvesting and analog data back-telemetry. The theoretical basis for a linear amplitude-modulated ultrasound echo modulation technique

TABLE II Performance Comparison Table

	[2]	[4]	[3]	This work
Link	Ultrasound	Optical	RF	Ultrasound
Back telemetry	AM Backscatter	Analog PPM	IR-UWB	AM Backscatter
Implant depth (mm)	8.8	_	20	50
Total Volume (mm ³)	0.8	0.004	<1	0.8
Encapsulated	Yes	No	Yes	Yes
Depth/Volume (mm ²)	11	_	20	62
Simultaneous Multi-mote	No	No	No	Yes
Technology (nm)	65	180	350	65
Total IC power (μW)	_	0.9	296^{*}	37.7
IC area (mm ²)	500×450	57×250	1050×1050	500×500
Wake-up time (μs)	3.3	15000	110	11
THD (dB)	_	$-16@0.5mV_{pp}$	_	-52/-44@10/20mVpp
Static nonlinearity (%)	-	$49^{\dagger}@6mV_{PP}$	-	$1.2@20mV_{PP}$
noise floor (μV_{rms})	180	15	3.78	5.3
Bandwidth (kHz)	5	10	12	5
LNA power (μW)	_	0.52	42.9	4
NEF/ PEF	_	4.07/16.6	6.6/78.4	5.87/34.55
Gain (dB)	0	30	53	24
†estimated				

^{*}after AC-to-DC

was introduced, achieving a 20-mV_{PP} linear range of the implant. A comparison with recently published fully integrated free-floating sub-mm³ neural recording implants is shown in Table 2. This work advances the noise performance of [2] by

 $34\times$ without sacrificing the implant volume. Compared with prior art [2]–[4], this work achieves the lowest nonlinearity at the highest input range, achieves a comparable NEF with that of the state-of-the-art, and improves the operating depth by >2.5×, resulting in the highest measured depth/volume ratio by ~ 3×. We demonstrate, for the first time to the best of our knowledge, simultaneous power-up and communication with two free-floating motes without requiring a specialized, e.g., beamformed, external transducer.

APPENDIX

PIEZO Γ VERSUS VOLTAGE LINEARITY

This section provides the derivation of (5) earlier introduced in Section III. The piezo is modeled as a thicknessmode resonating three-port network, shown in Fig. 6(a), whose input–output port relationships are well described by [22]

$$\begin{bmatrix} F_1 \\ F_2 \\ V_3 \end{bmatrix} = \mathbf{P} \begin{bmatrix} v_1 \\ v_2 \\ I_3 \end{bmatrix} = \begin{bmatrix} m & n & p \\ n & m & p \\ p & p & r \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ I_3 \end{bmatrix}$$
(8)

$$\begin{bmatrix} F_1 \\ F_2 \\ V_3 \end{bmatrix} = \begin{bmatrix} \frac{Z_0 A}{j \tan(\beta l)} & \frac{Z_0 A}{j \sin(\beta l)} & \frac{h_{33}}{j \omega} \\ \frac{Z_0 A}{j \sin(\beta l)} & \frac{Z_0 A}{j \tan(\beta l)} & \frac{h_{33}}{j \omega} \\ \frac{h_{33}}{j \omega} & \frac{h_{33}}{j \omega} & \frac{1}{j \omega C_0} \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ I_3 \end{bmatrix}$$
(9)

Ports 1 and 2 are acoustical, and Port 3 is the electrical port of the piezo. Table 1 describes the parameters used in (9). The acoustic impedance seen into Port 1, while Ports 2 and 3 are, respectively, terminated by Z_B and Z_E [Fig. 6(b)], is given by

$$Z_1 = \frac{p^2(2n - 2m - Z_B) + (Z_E + r)(m^2 - n^2 + mZ_B)}{(Z_E + r)(m + Z_B) - p^2}.$$
 (10)

Therefore, Γ defined as $\Gamma = (Z_1 - Z_B)/(Z_1 + Z_B)$ becomes

$$\Gamma = \frac{2p^2(n-m) + (Z_E + r)(m^2 - n^2 - Z_B^2)}{2p^2(n-m-Z_B) + (Z_E + r)((m+Z_B)^2 - n^2)}.$$
 (11)

Rearranging terms and noting that $m^2 - n^2 = (Z_o A)^2 \gg Z_B^2$, (11) can be simplified to

$$\Gamma \approx \frac{Z_E + Z_{3,\text{NL}}}{Z_E + 2Z_B \left(\frac{mr - p^2}{m^2 - n^2}\right) + Z_{3,\text{NL}}}$$
(12)

where $Z_{3,NL}$ is the impedance seen into Port 3 when Ports 1 and 2 are acoustically unloaded [Fig. 6(d), $Z_B = 0$]. In fact, for nonzero acoustic termination impedance at Ports 1 and 2 [Fig. 6(c)]

$$Z_3 = r - \frac{2p^2}{m + n + Z_B}.$$
 (13)

The series-resonant frequency (f_s) is defined as the frequency at which the impedance seen into the electrical port of an acoustically unloaded piezo is real. That is, at f_s , $Z_{3,NL} = 0$ $[Z_{3,\text{NL}} = Z_3(atZ_B = 0)$ is purely imaginary], and (12) further simplifies to

$$\Gamma \approx \frac{Z_E}{Z_E + 2Z_B \left(\frac{mr - p^2}{m^2 - n^2}\right)}.$$
(14)

Moreover, at f_s , the piezo resonator is modeled by a voltage source and a series resistance, shown in Fig. 5(b), whose value is given by

$$R_{S} = \operatorname{Re}\{Z_{3}\} = \operatorname{Re}\left\{r - \frac{2p^{2}}{m+n+Z_{B}}\right\} \approx \frac{2Z_{B}p^{2}}{(n+m)^{2}}.$$
 (15)

Dividing the second term in the denominator of (14) by (15) results in $(mr/p^2 - 1)((m + n)/(m - n))$, which is equal to 1 at f_s , because

$$\frac{m+n}{m-n} = -\cot^2\left(\frac{\beta l}{2}\right) \tag{16}$$

and

$$\frac{mr}{p^2} - 1 = \frac{\beta l}{k_T^2 \tan(\beta l)} - 1.$$
 (17)

Given at f_s [22],

$$\frac{\tan(\beta l/2)}{\beta l/2} = \frac{1}{k_T^2} = \frac{1+k^2}{k^2}$$
(18)

(17) can be further simplified to

$$\frac{nr}{p^2} - 1 = -\tan^2\left(\frac{\beta l}{2}\right). \tag{19}$$

Therefore, the second term in the denominator of (14) and R_S given by (15) are equal. That is

$$R_S = \frac{2Z_B p^2}{(n+m)^2} = 2Z_B \left(\frac{mr - p^2}{m^2 - n^2}\right).$$
 (20)

Therefore, (14) can be rewritten as

$$\Gamma \approx \frac{Z_E}{Z_E + R_S} \propto V_3. \tag{21}$$

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Dr. Muller is a member of the technical program committees for IEEE ISSCC, and has previously served on the committees of IEEE CICC and BioCAS. She is a member of the Solid-State Circuits Society, the Women in Circuits, and the Society for Neuroscience. She was a recipient of the National Academy of Engineering Gilbreth Lectureship, the Chan-Zuckerberg Biohub Investigatorship, the Keysight Early Career Professorship, and the NSF CAREER Award. She has also served as a Guest Editor for the IEEE JOURNAL OF SOLID-STATE CIRCUITS.